Welcome To

ISSCC 2014
SESSION 3

RF Techniques

Polar Antenna Impedance Detection and Tuning for Efficiency Improvement in a 3G/4G CMOS Power Amplifier

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TOSHIBA
Leading Innovation

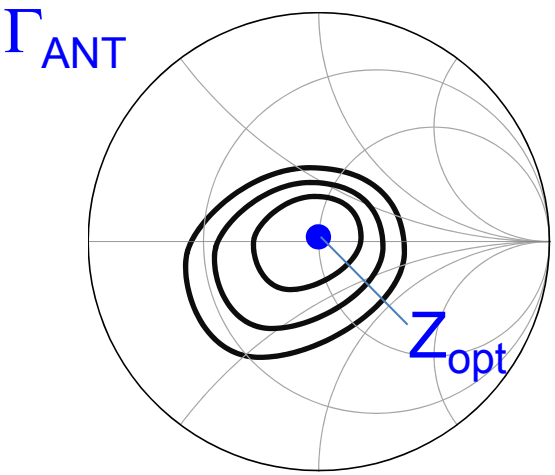
Outline

- Introduction
- Polar antenna impedance detection and tuning
- Circuit design and implementation
- Measurement results
- Conclusions

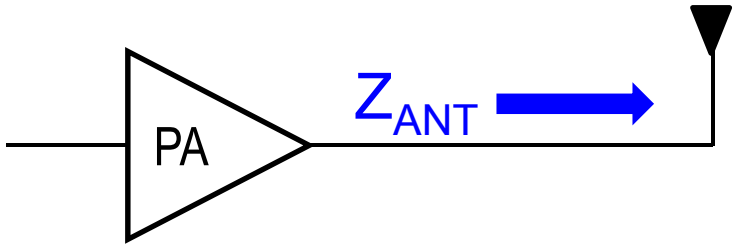
Backgrounds

- Effective efficiency of power amplifier is important for a longer battery life.
- Impedance mismatch is critical to the effective efficiency.

Load Dependency



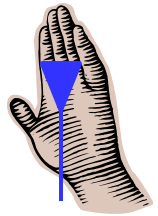
$Z_{opt} = Z_{ANT} = 50\Omega$

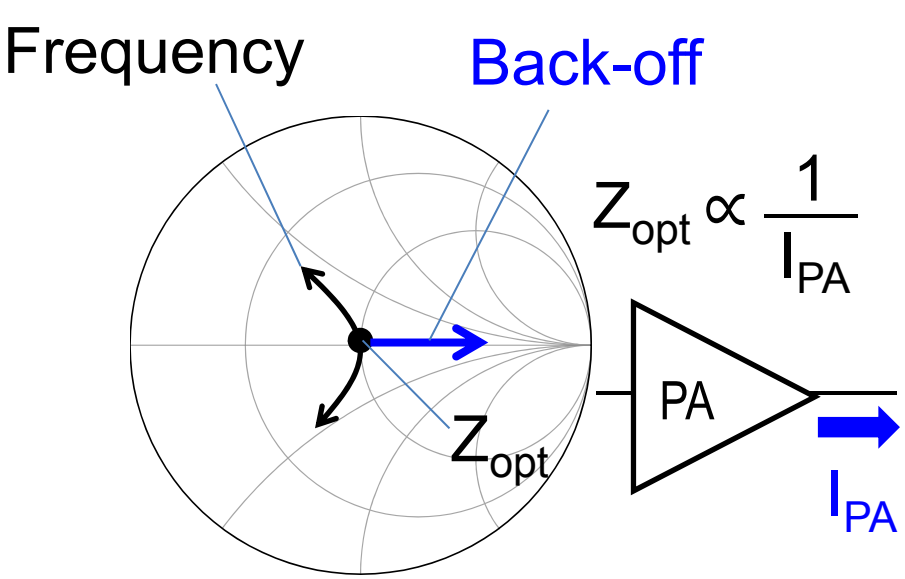


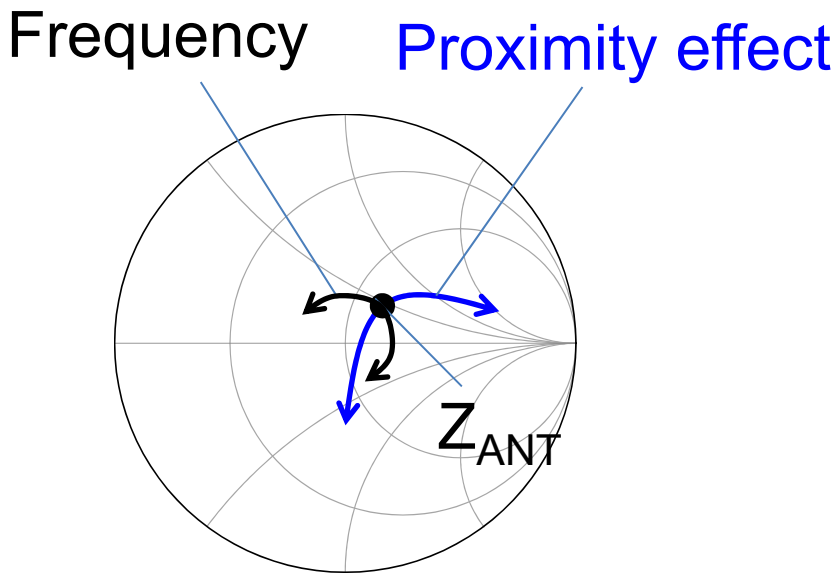
$Z_{opt} = Z_{ANT}$

Impedance Mismatch

- PA: Z_{opt}
  - Frequency
  - Back-off
- Antenna: Z_{ANT}
  - Frequency
  - Proximity effect







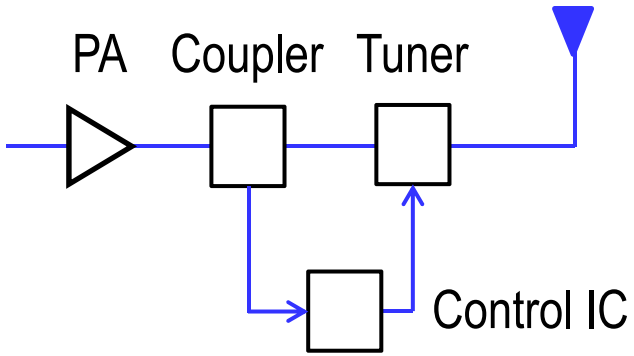
Antenna Impedance Tuning

Conventional

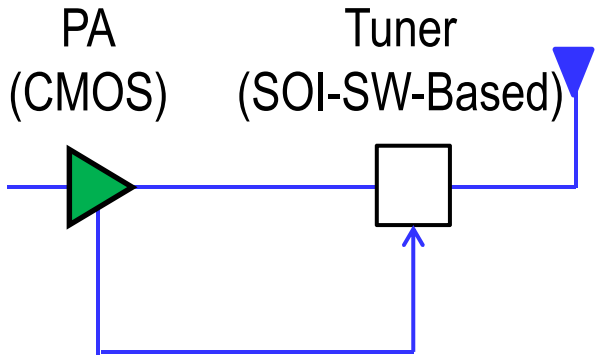
- Z_{ANT} = 50Ω only
- Slow (exhaustive search)
- Constant envelope
- Costly, large footprint

Proposed

- Z_{opt} for a PA
- Fast (successive approx.)
- Non-constant envelope
- Cost-effective, small footprint

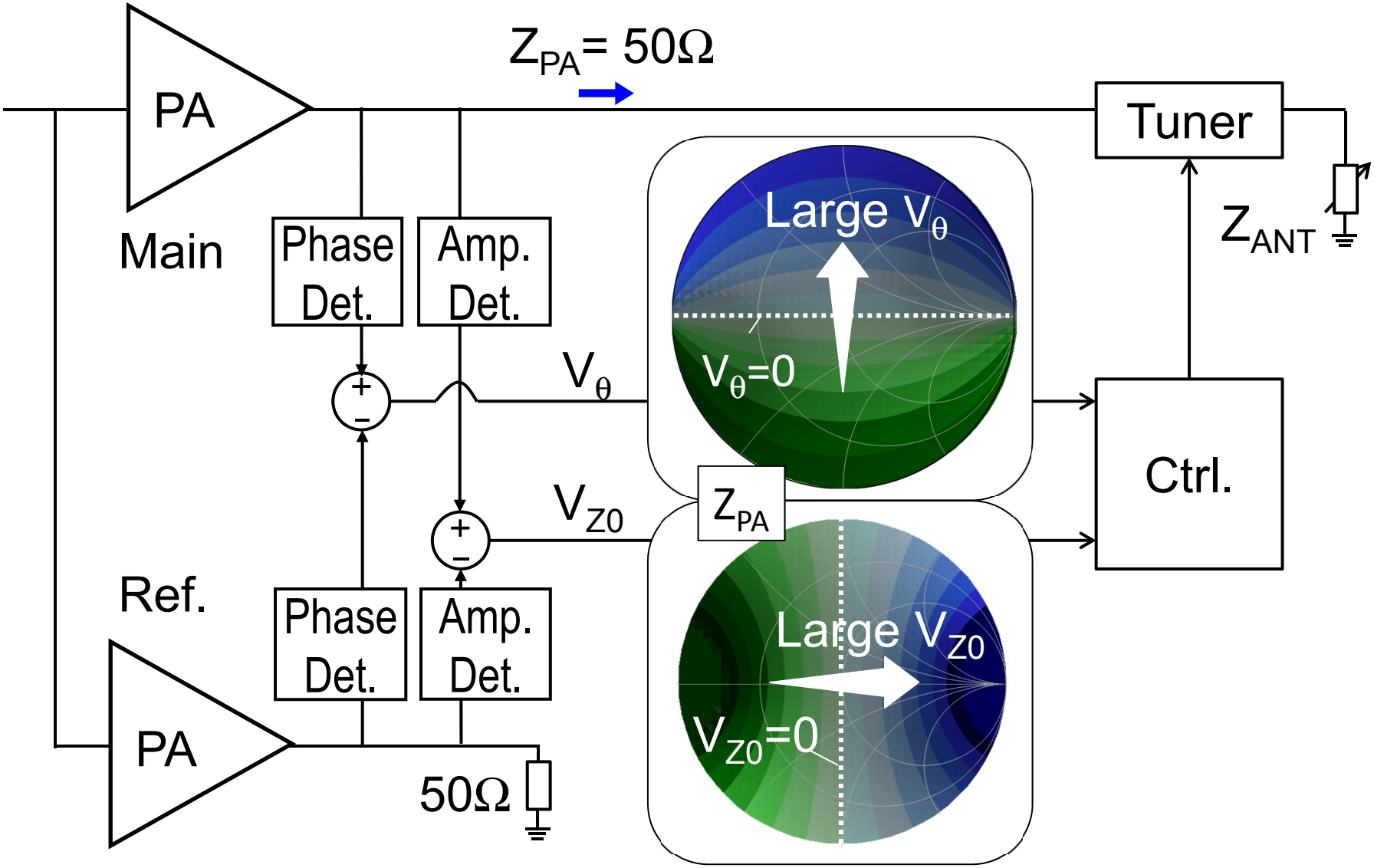


Scalar VSWR
ISSCC2009 [2]

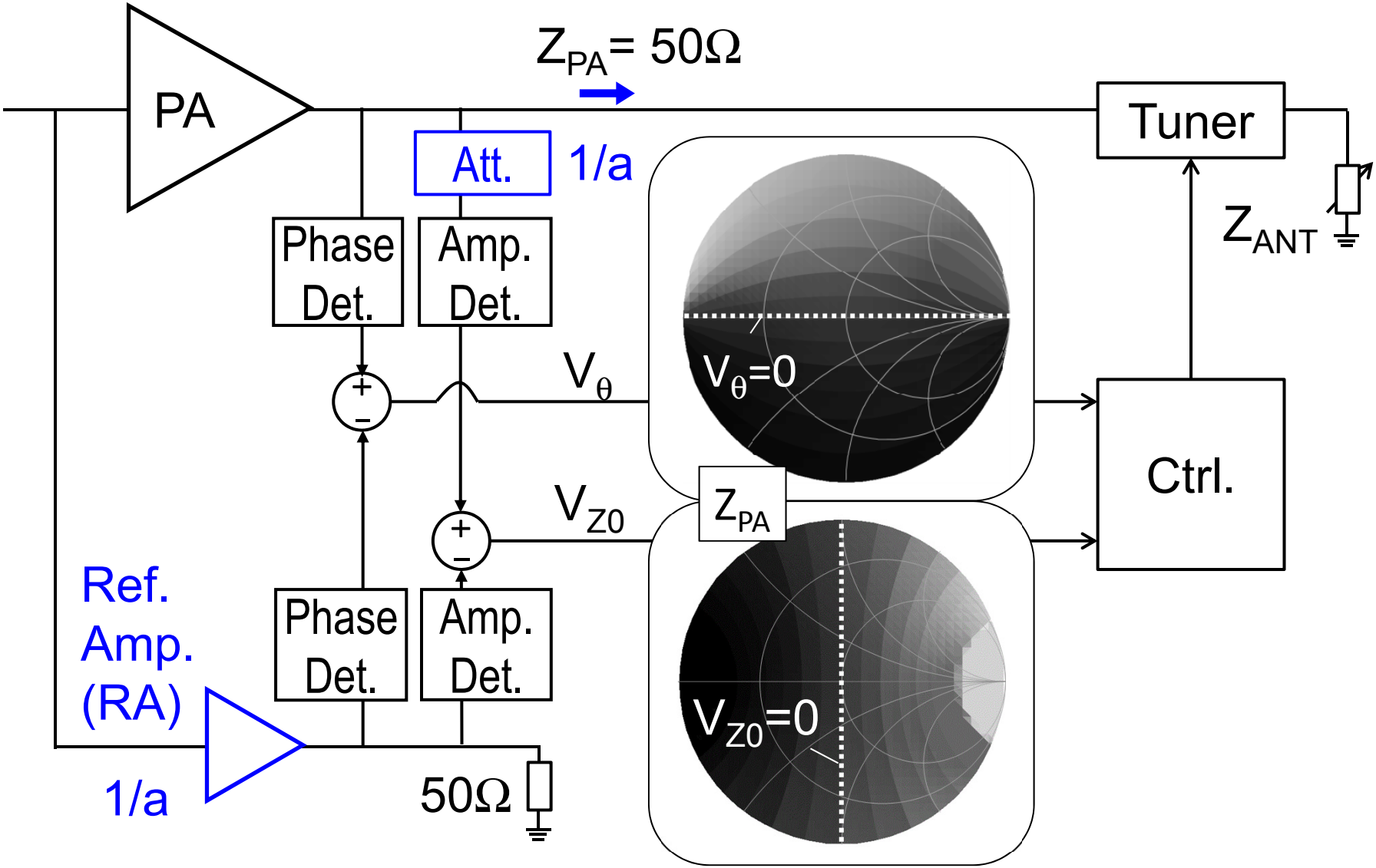


Polar impedance

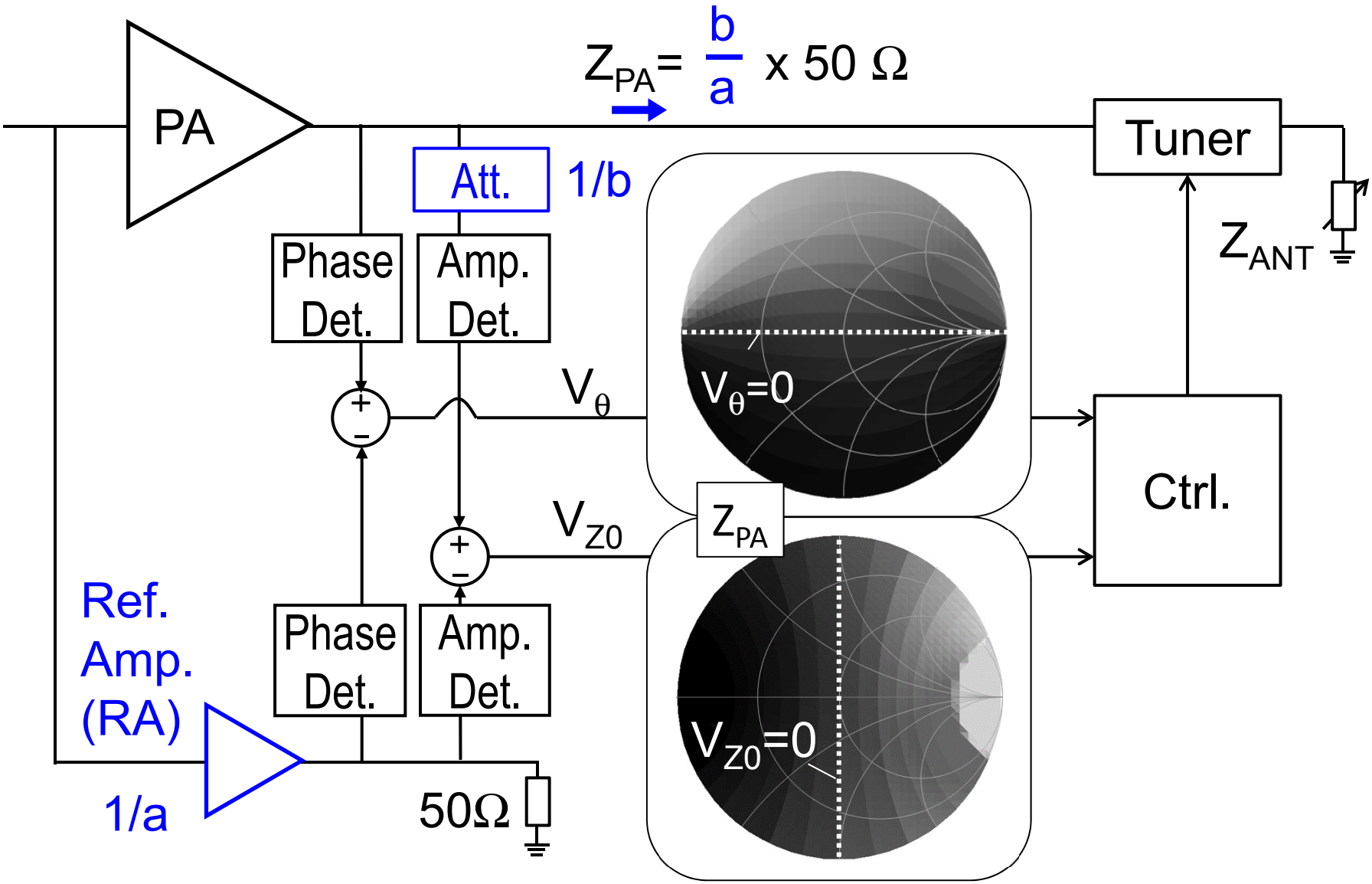
Concept of Proposed Scheme



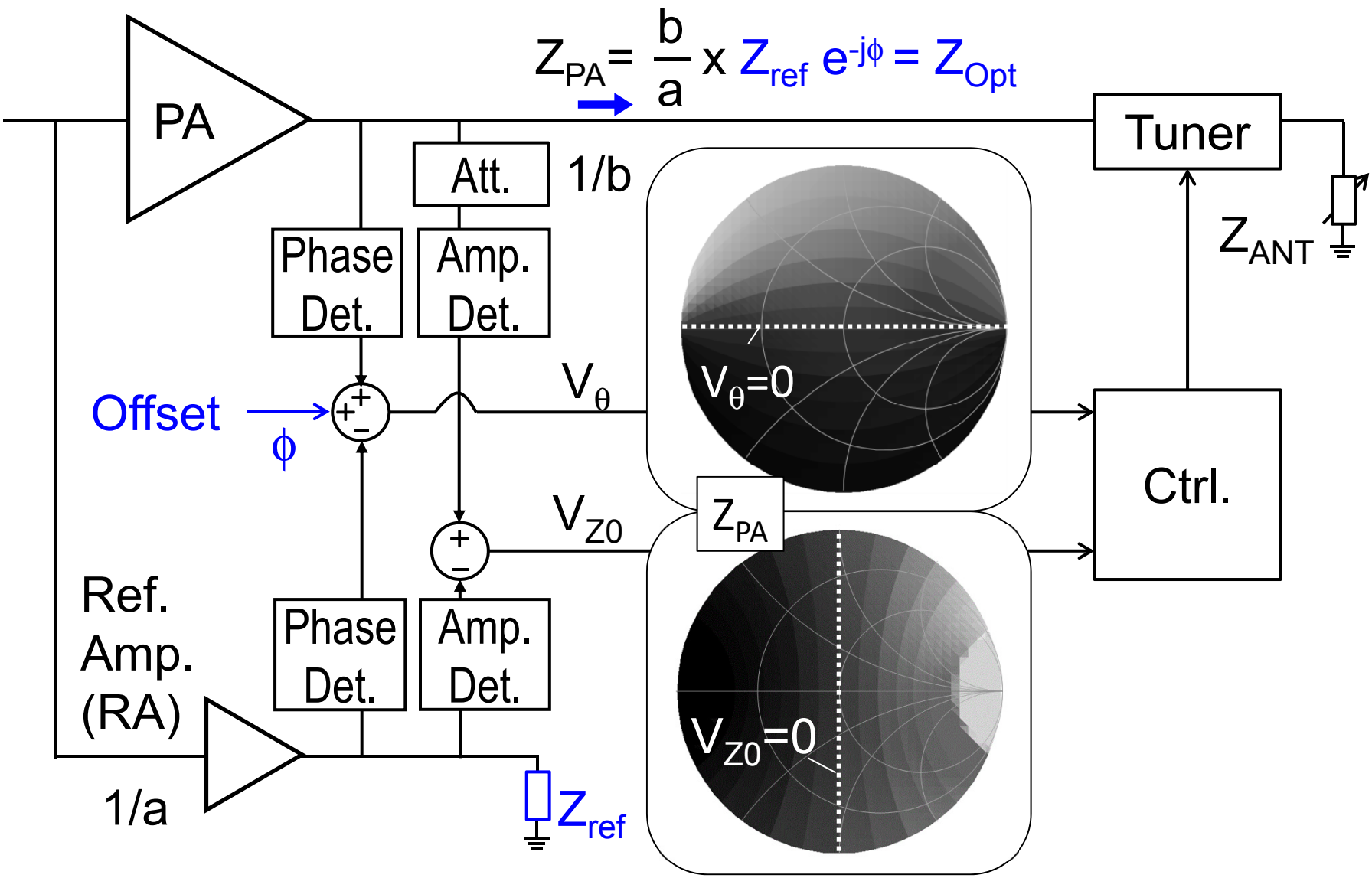
Reference Scaling



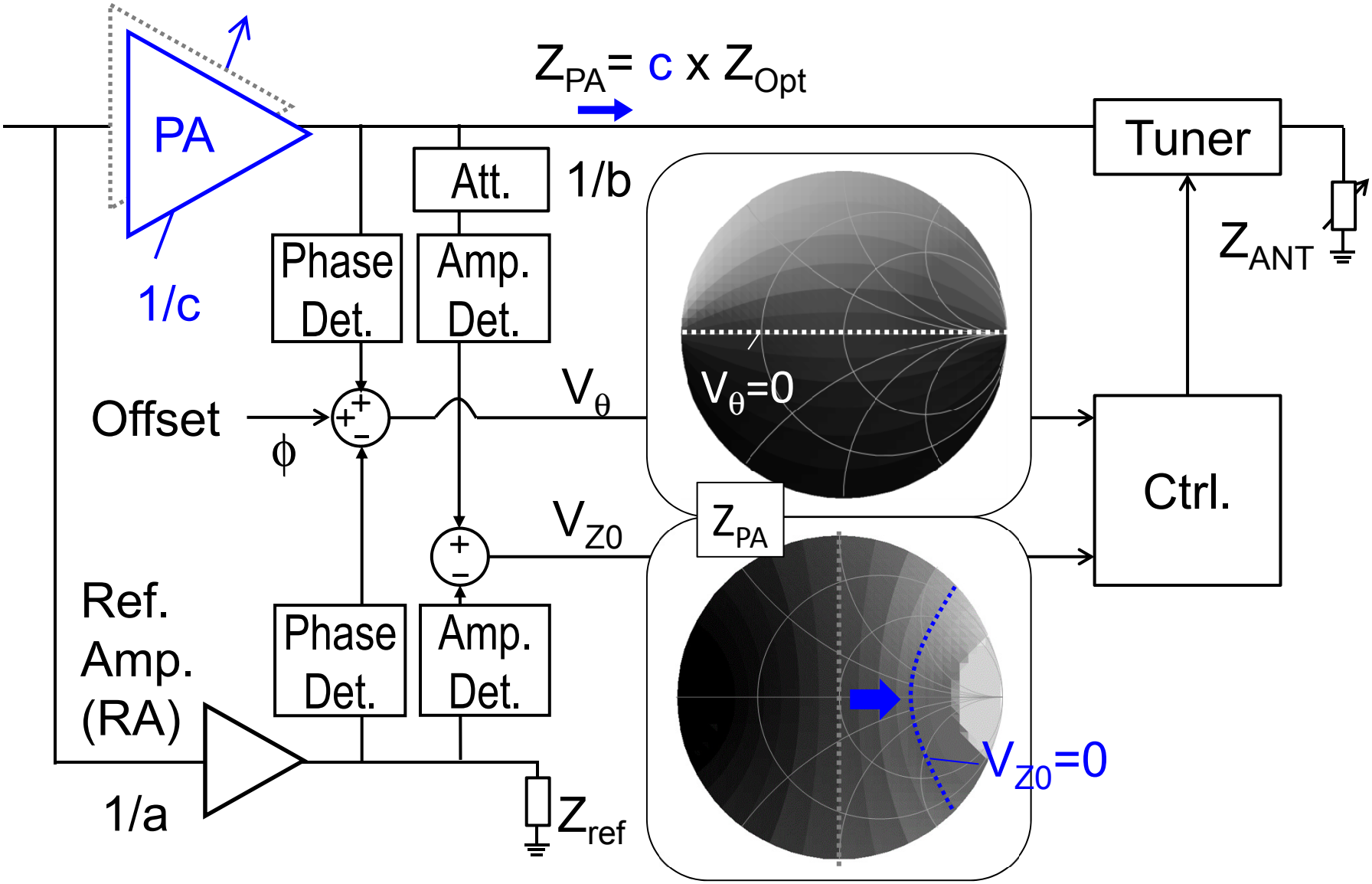
Magnitude Scaling



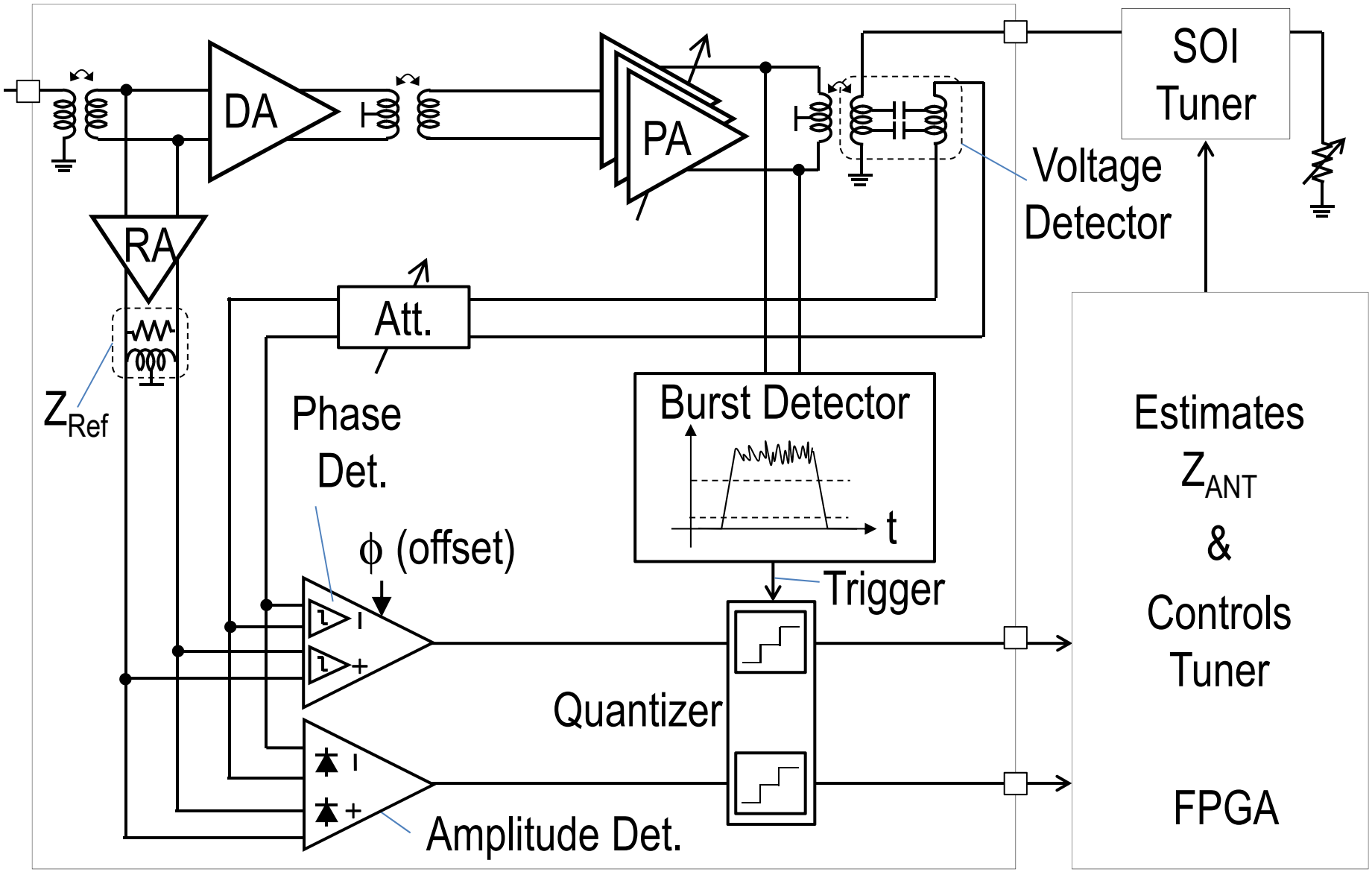
General Impedance Tuning



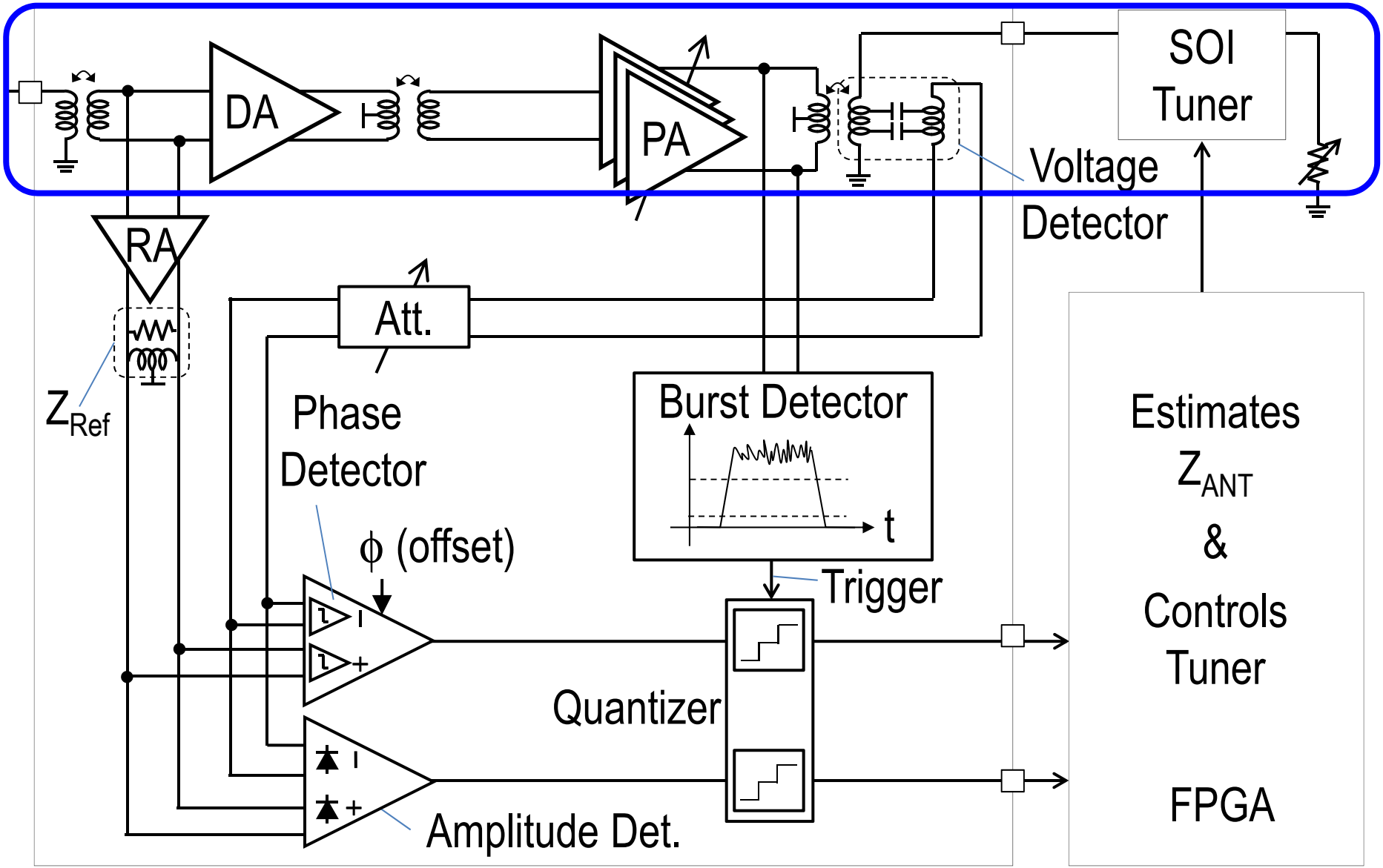
Back-off Efficiency Improvement



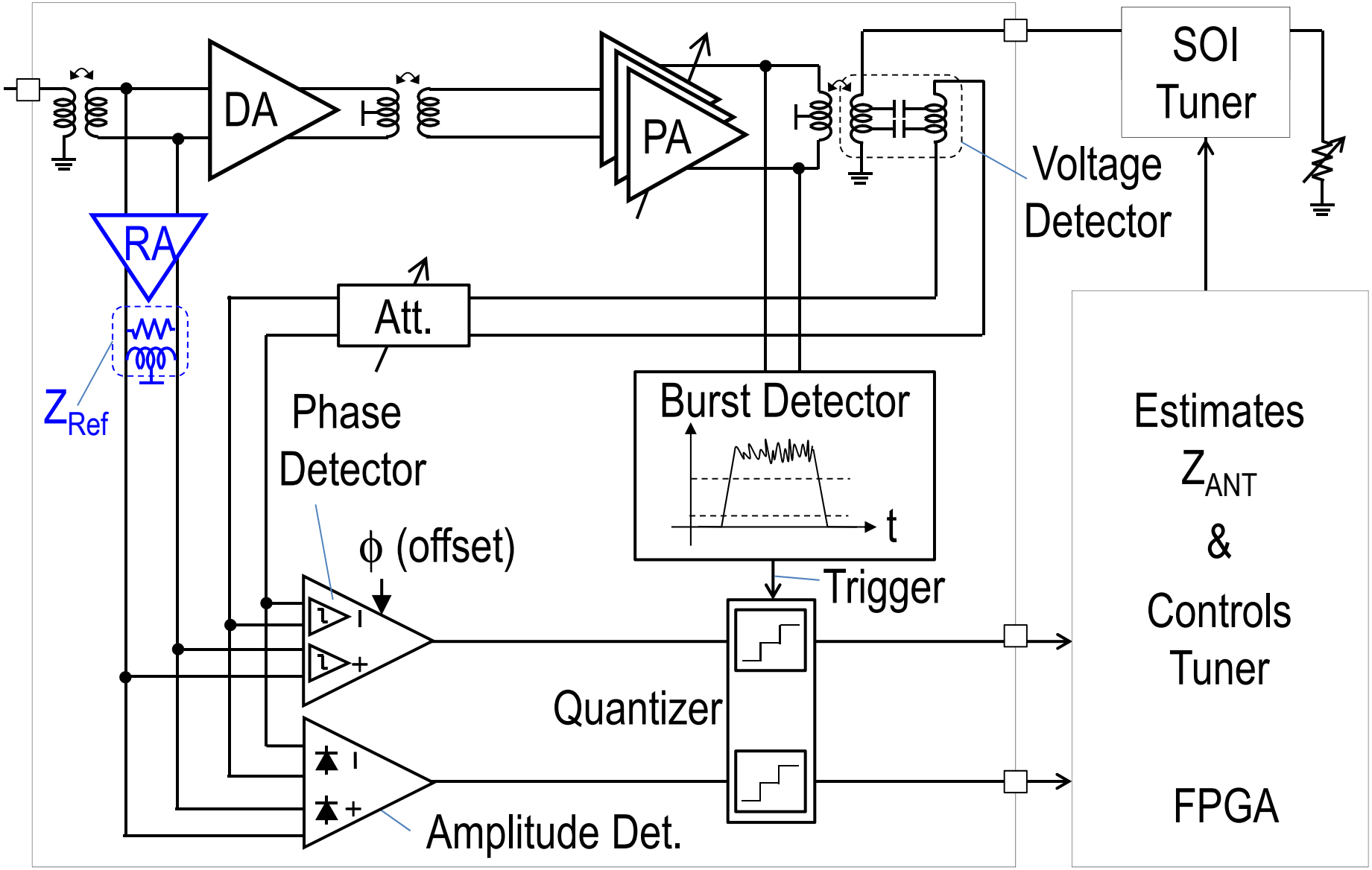
Detailed Block Diagram



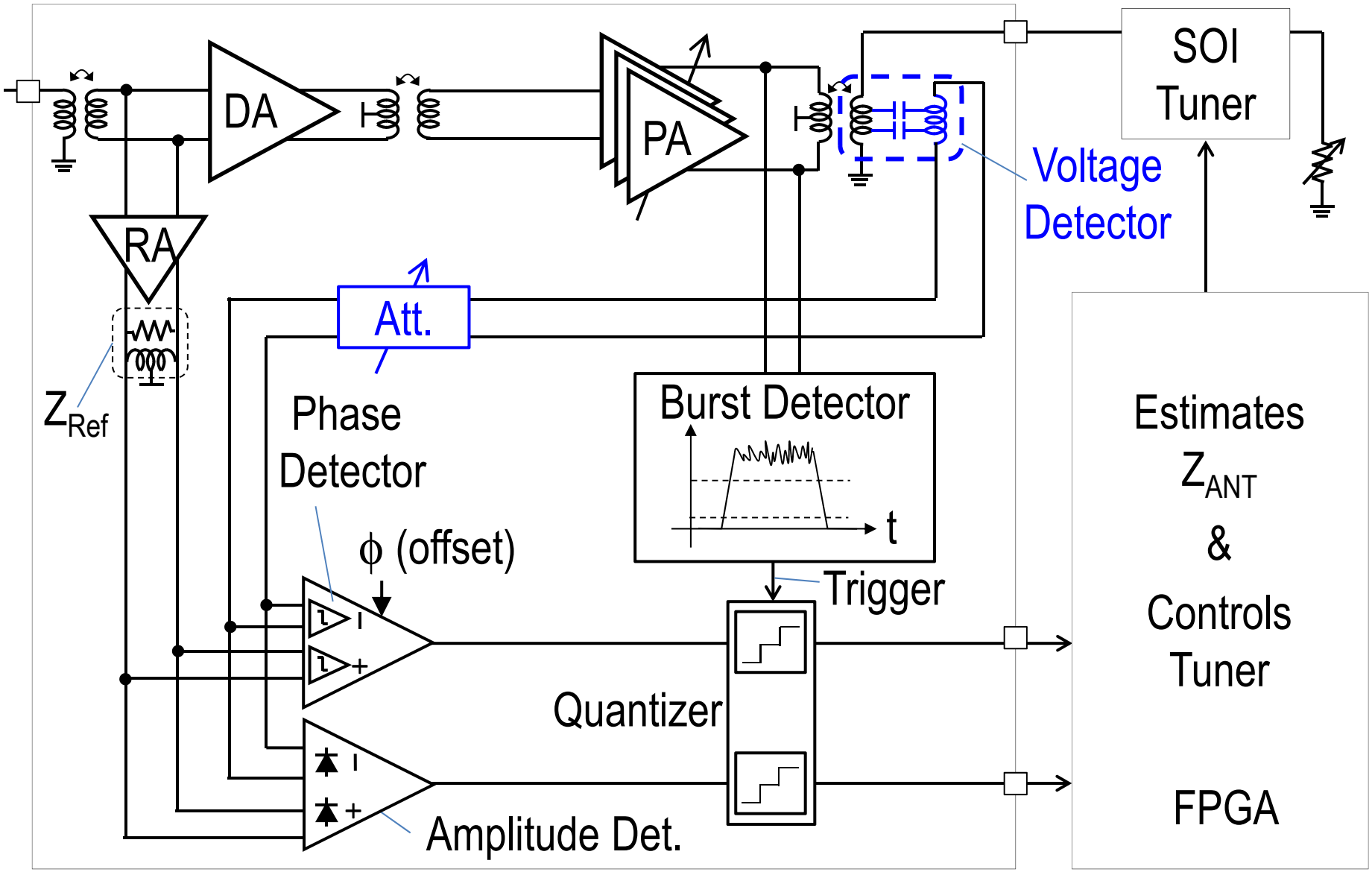
Detailed Block Diagram



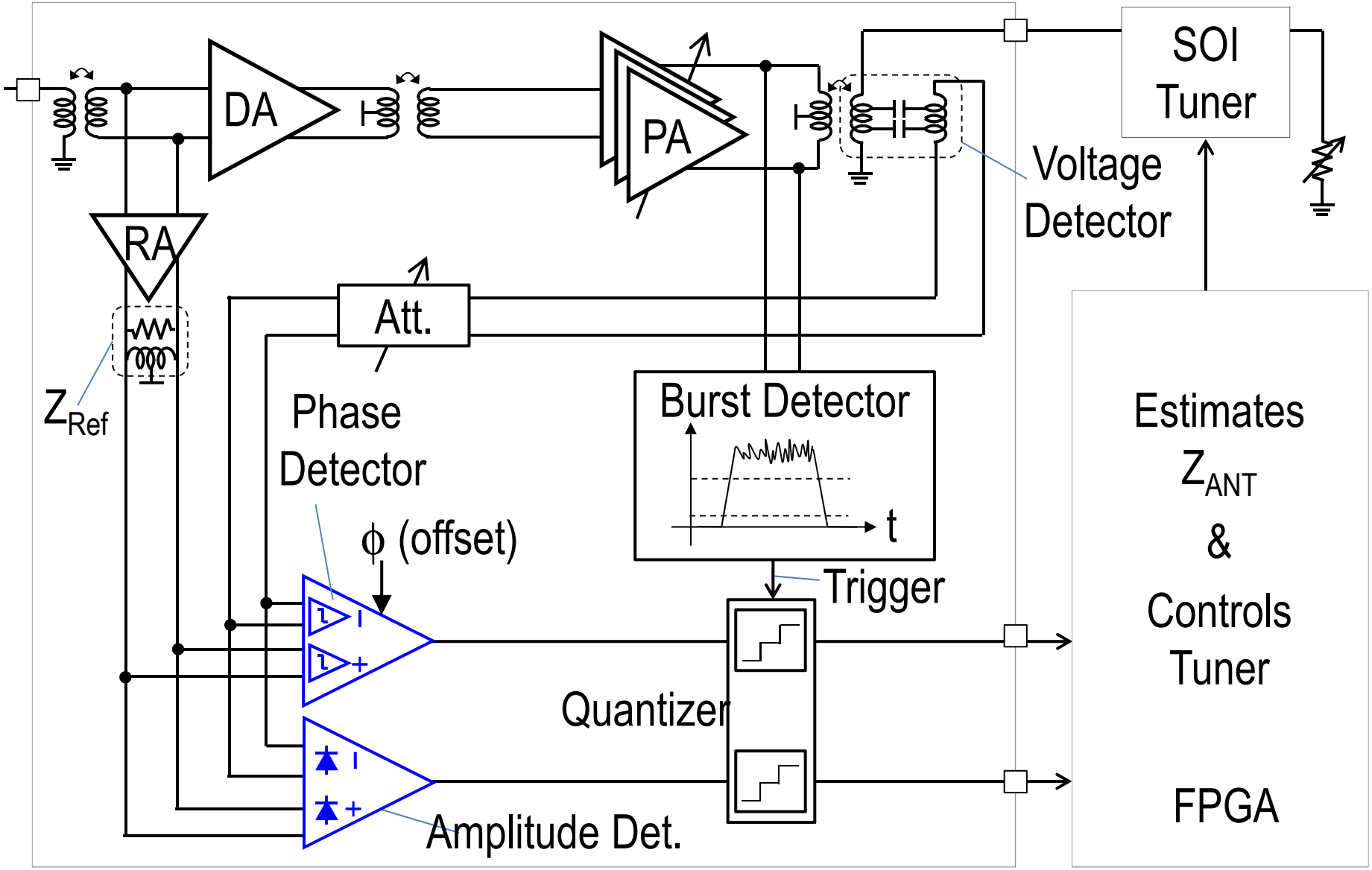
Detailed Block Diagram



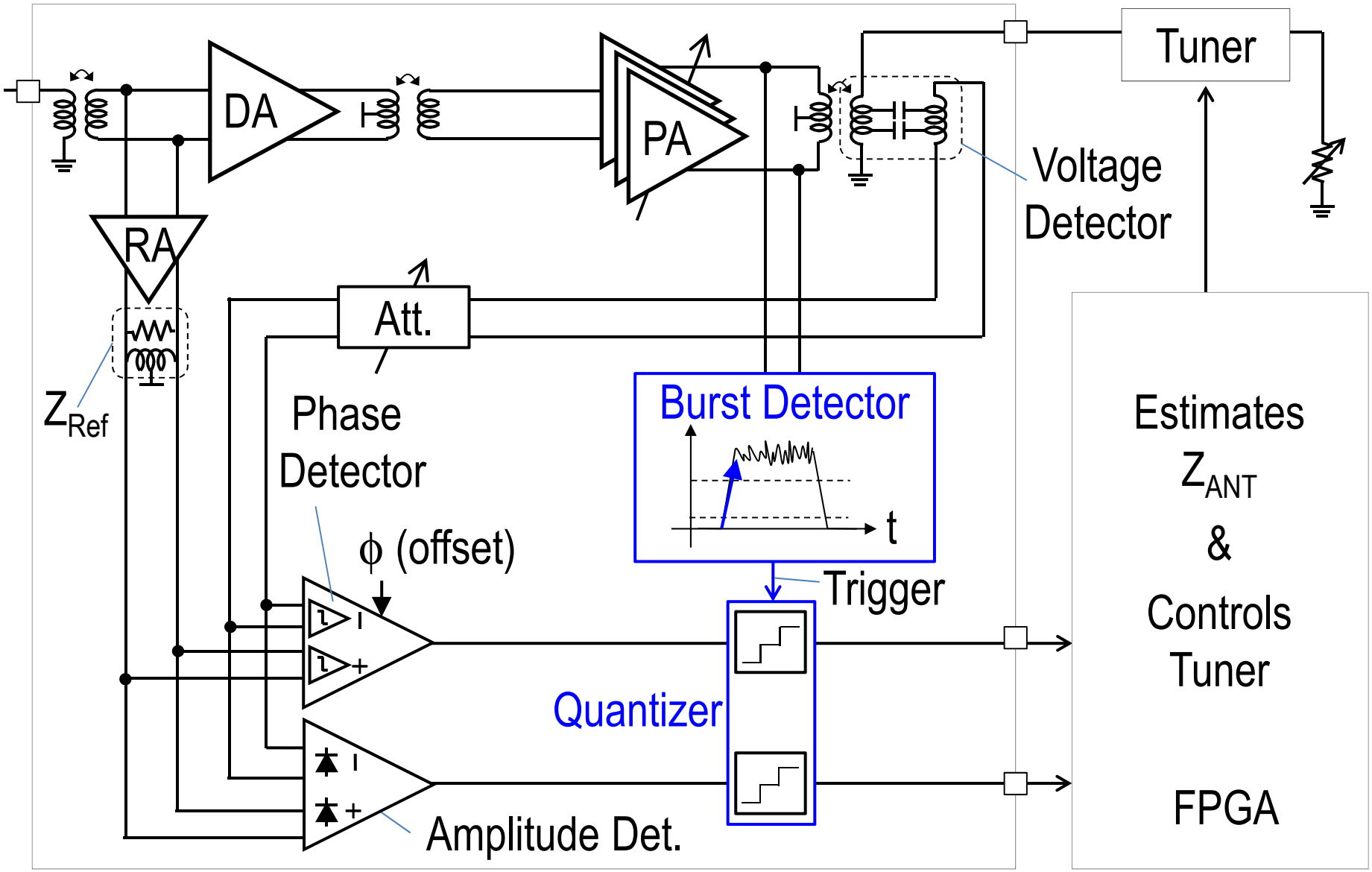
Detailed Block Diagram



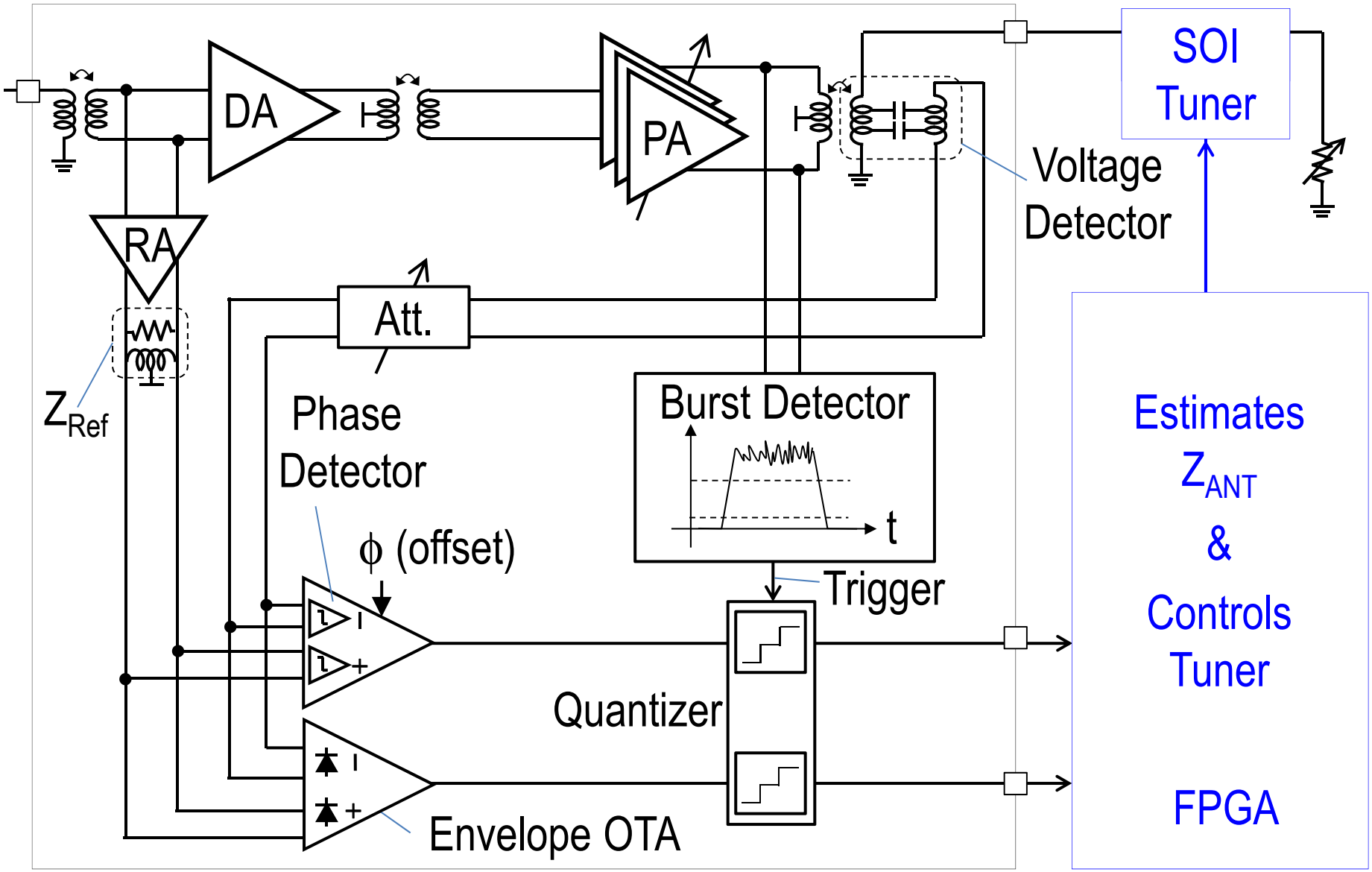
Detailed Block Diagram



Detailed Block Diagram



Detailed Block Diagram



PA-Closed Loop

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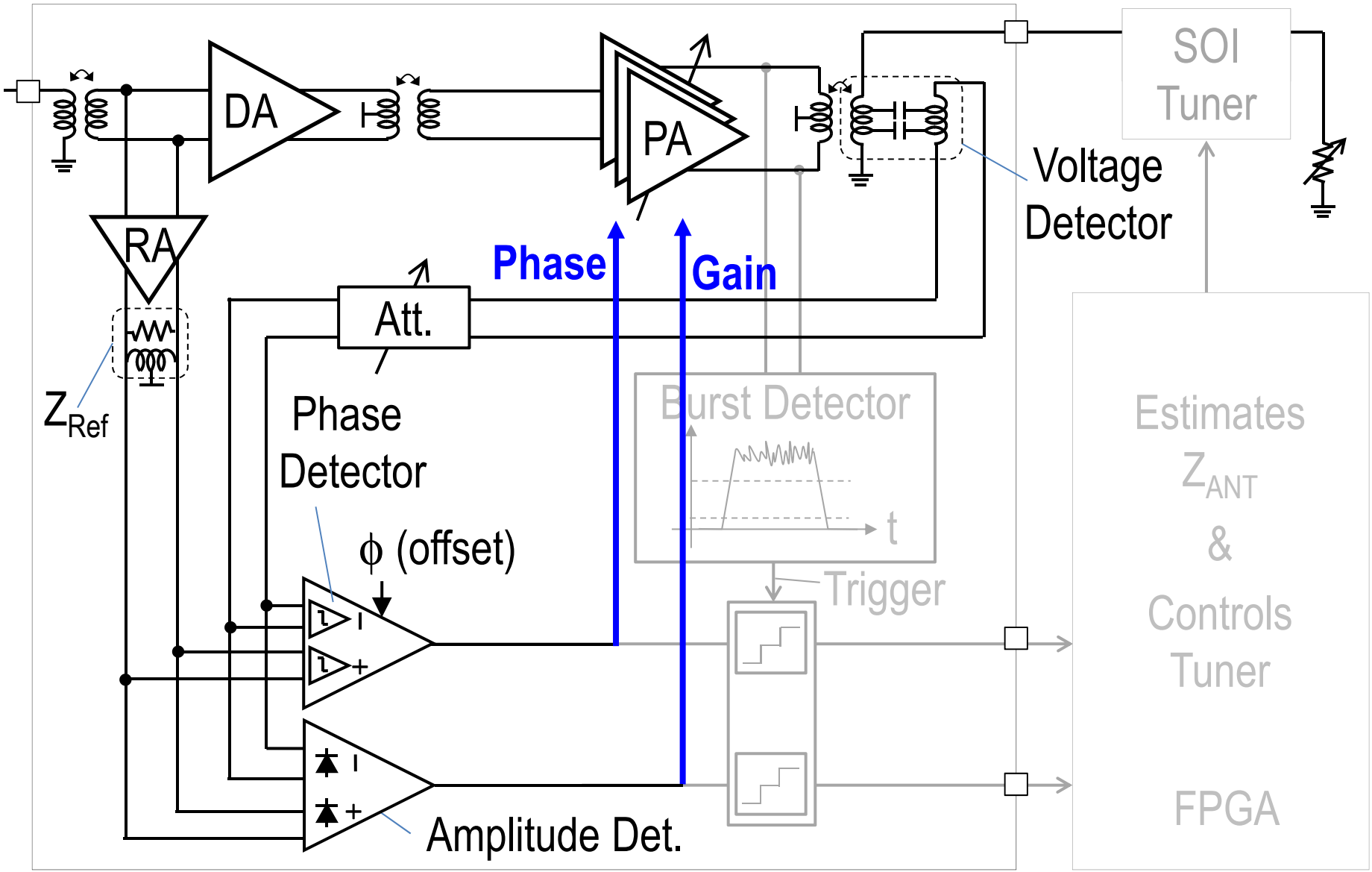
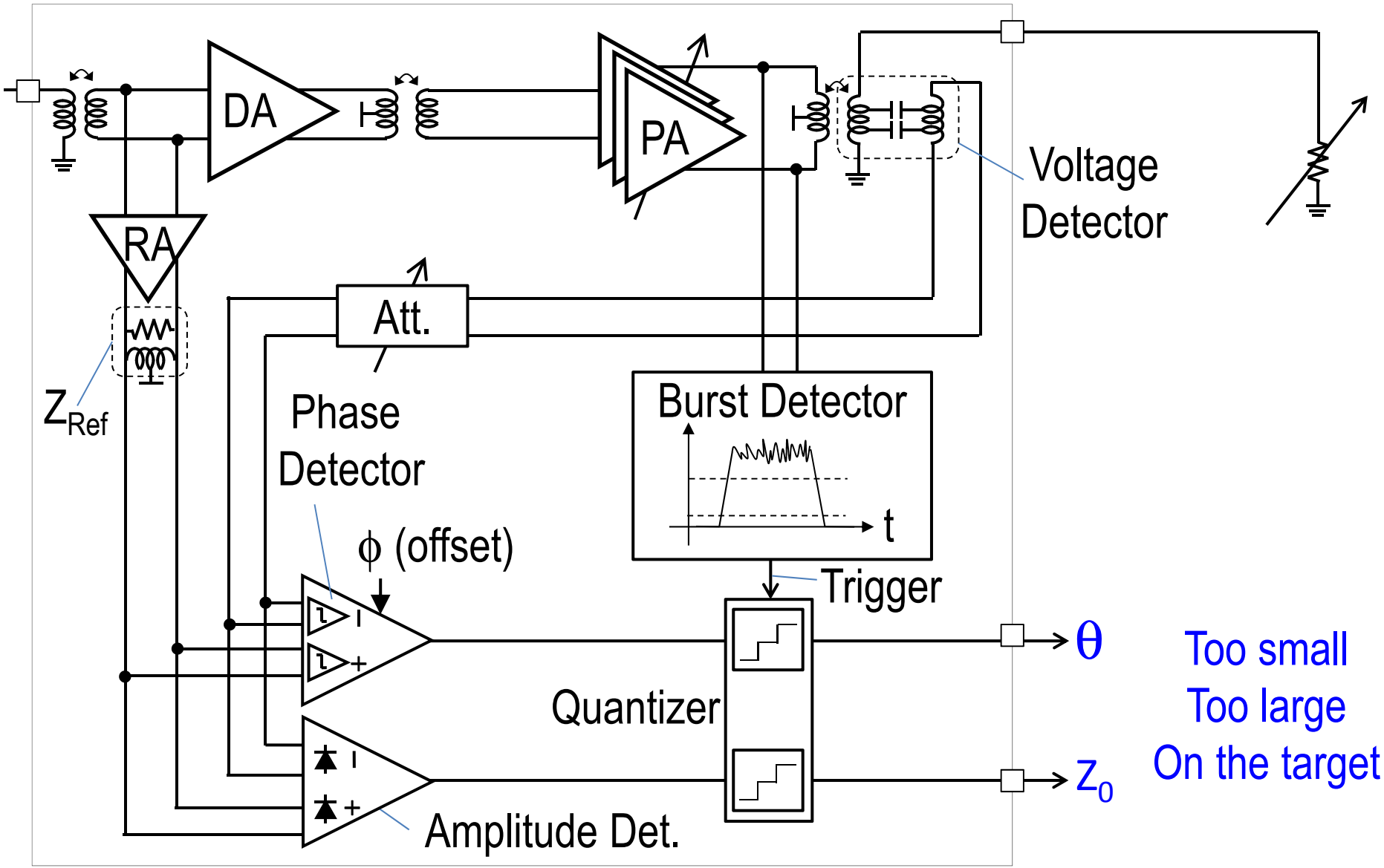
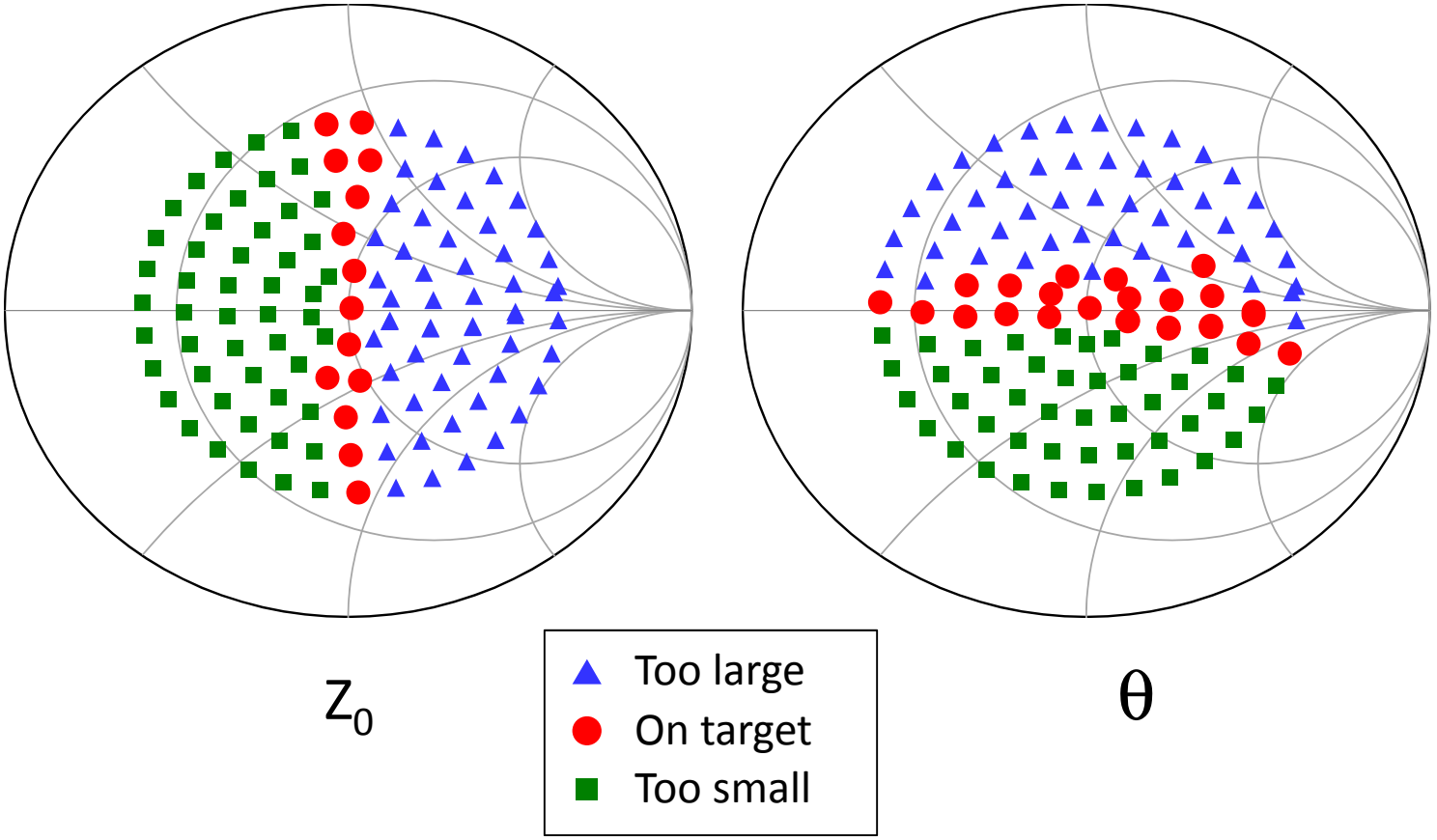


Impedance Measurement



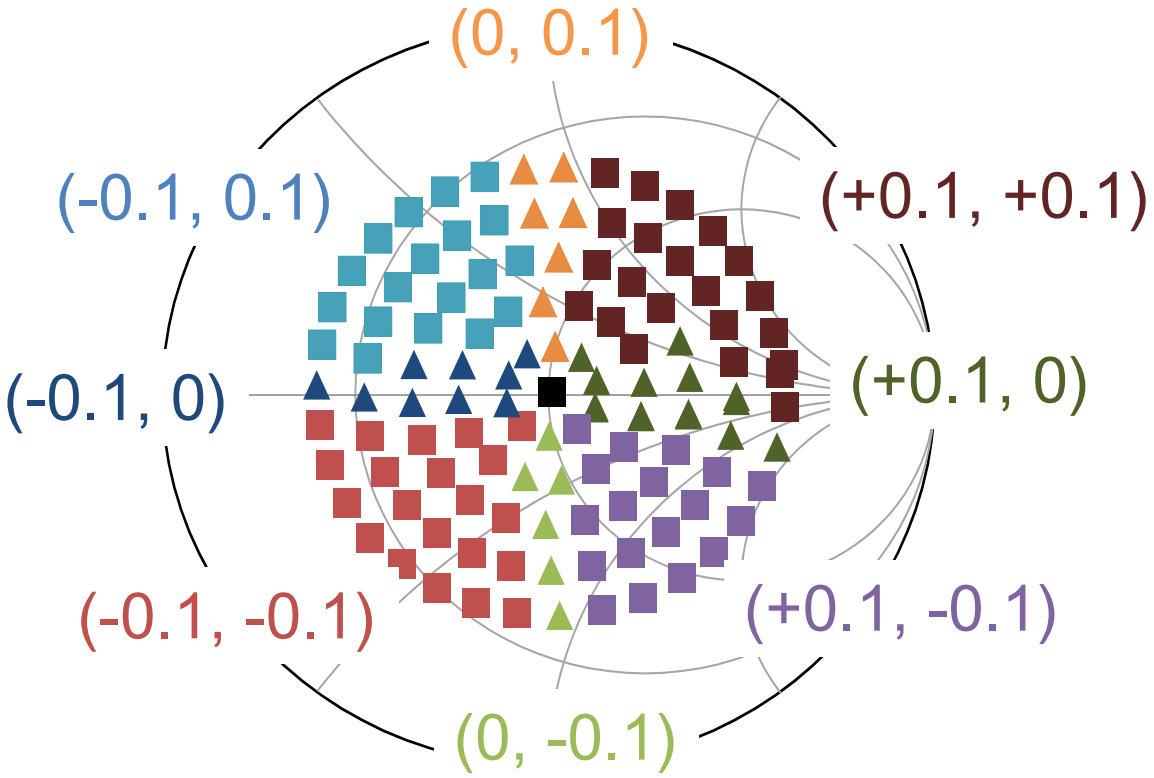
Impedance Measurement Result

- Measures 50Ω accurately.

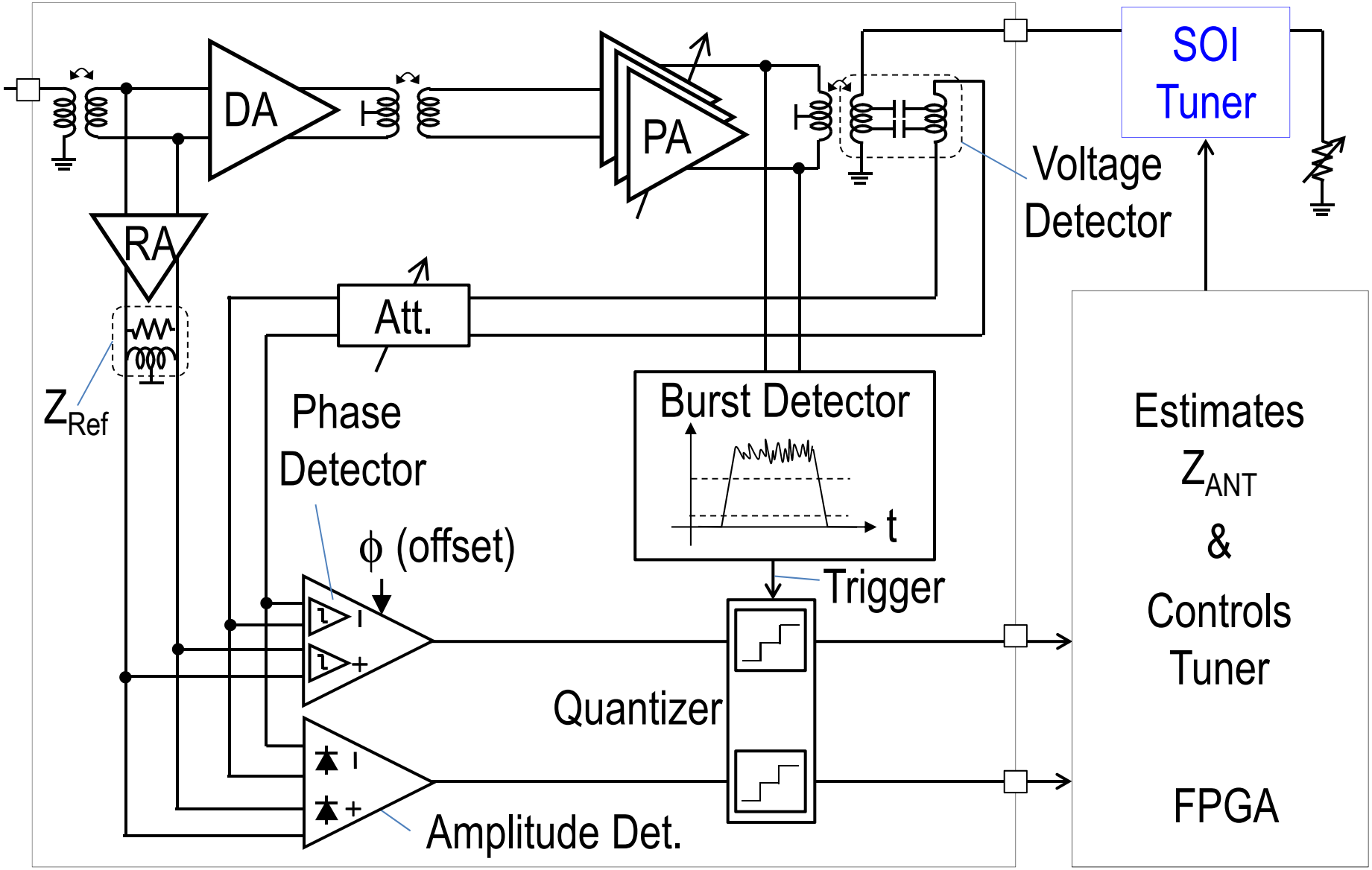


Tuner Setting Update

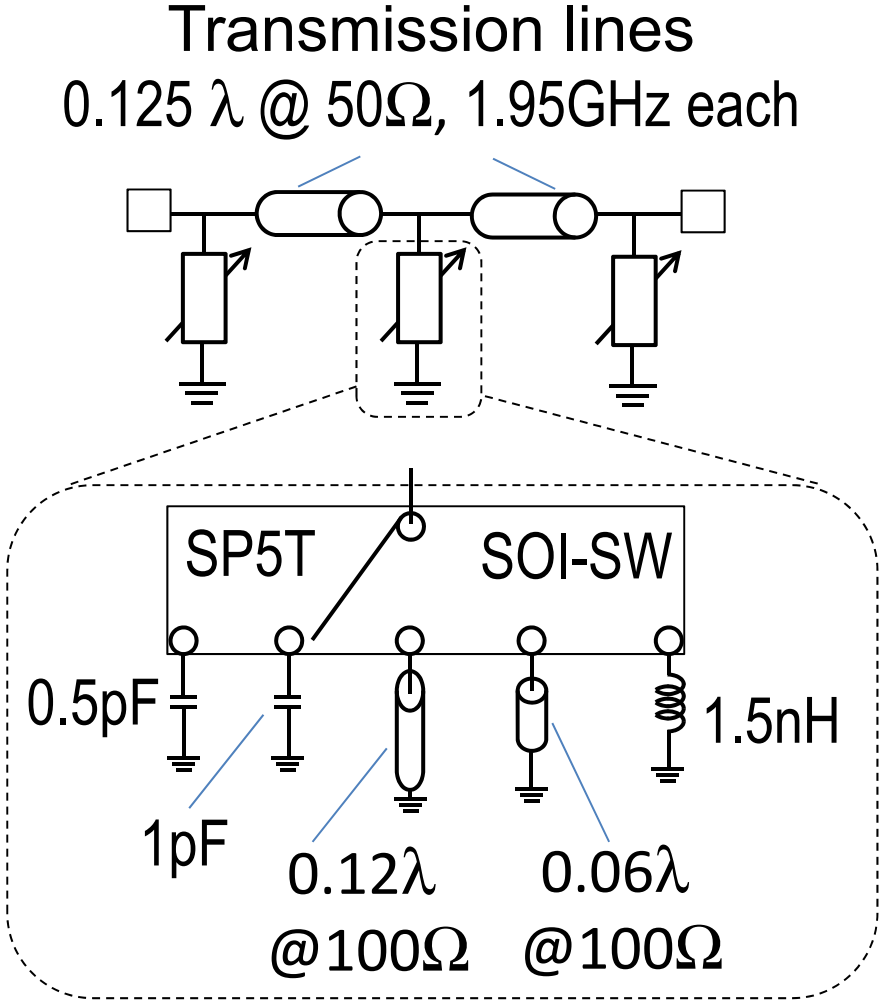
- Tuner setting is updated according to the quantized result.

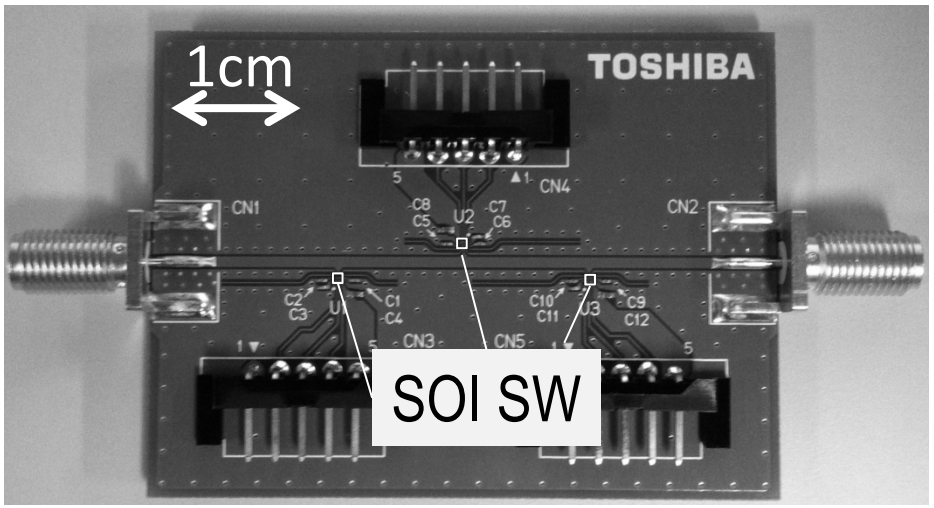


Detailed Block Diagram



SOI-SW Based Tuner Prototype

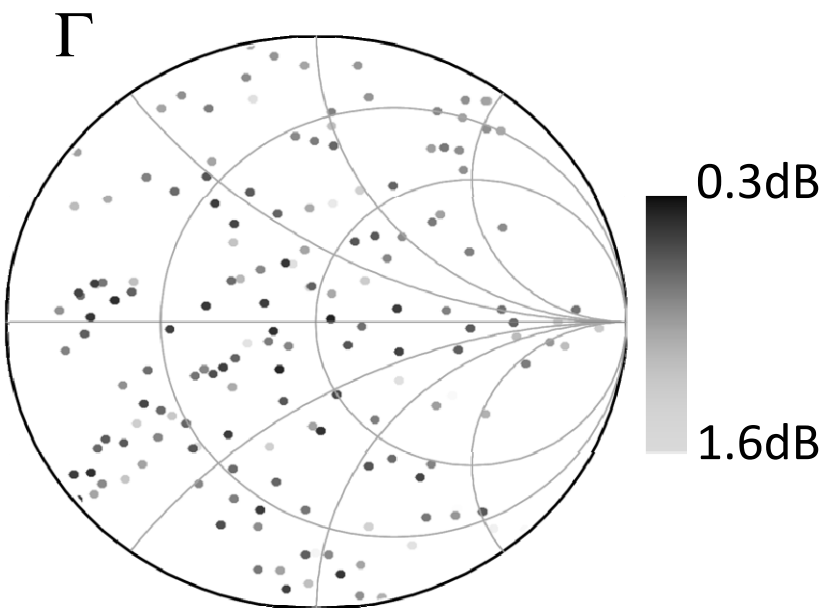


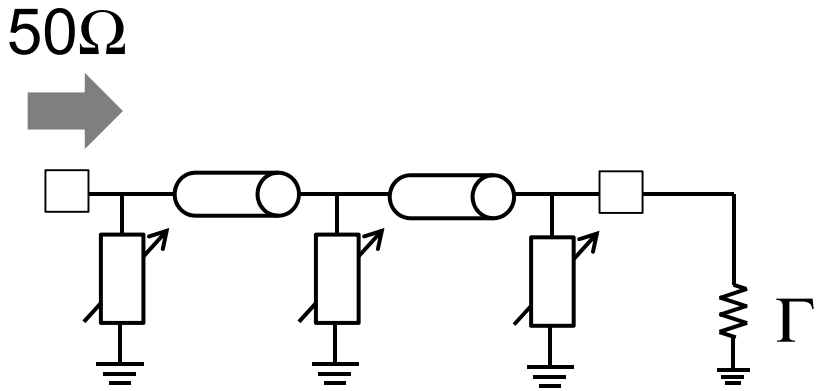


- 180nm SOI CMOS
- SP5T
- 1.08mm x 0.97mm (package)

Tuner Measurement Results

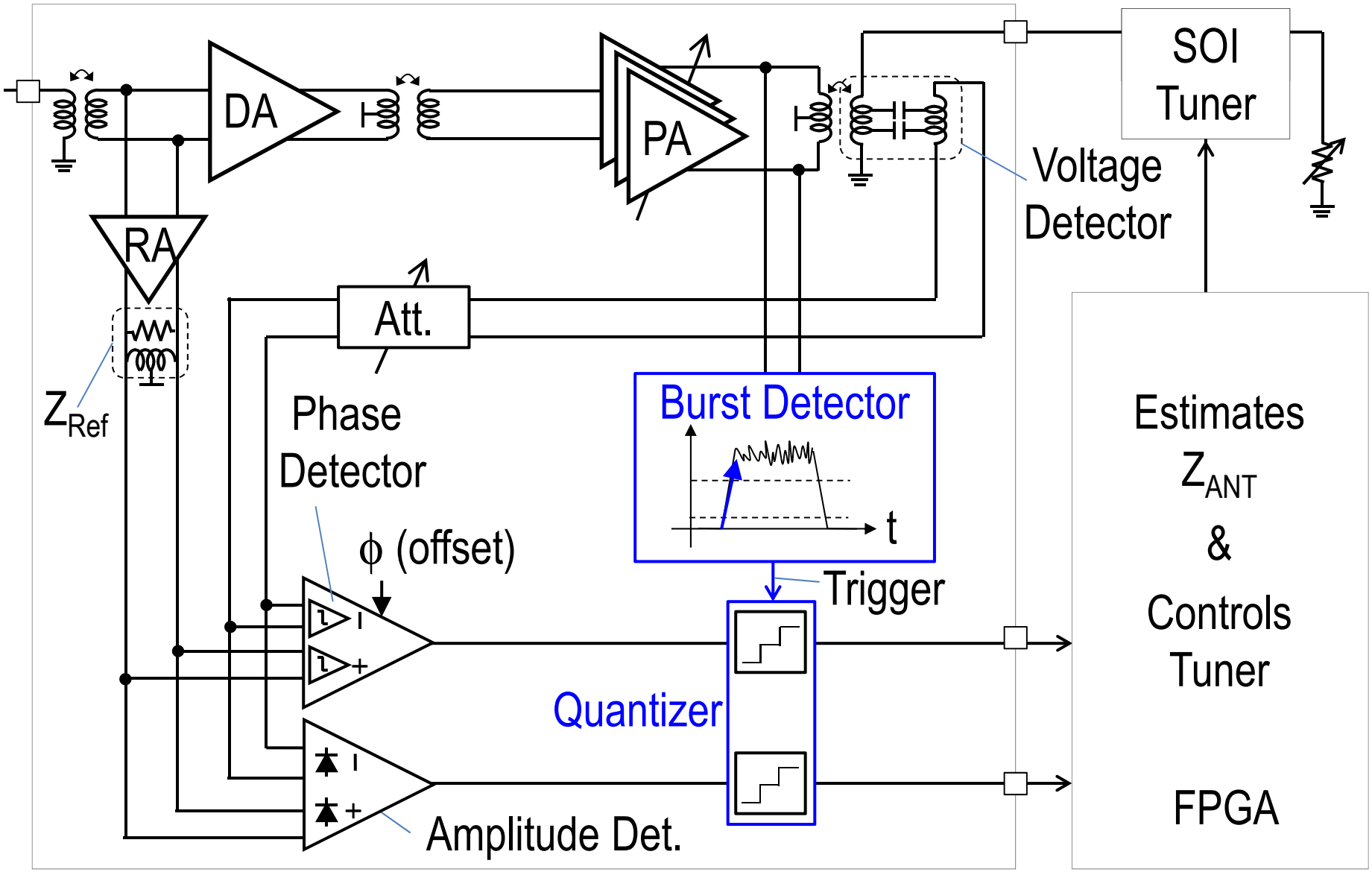
- The loss ranges from 0.3dB to 1.6dB.





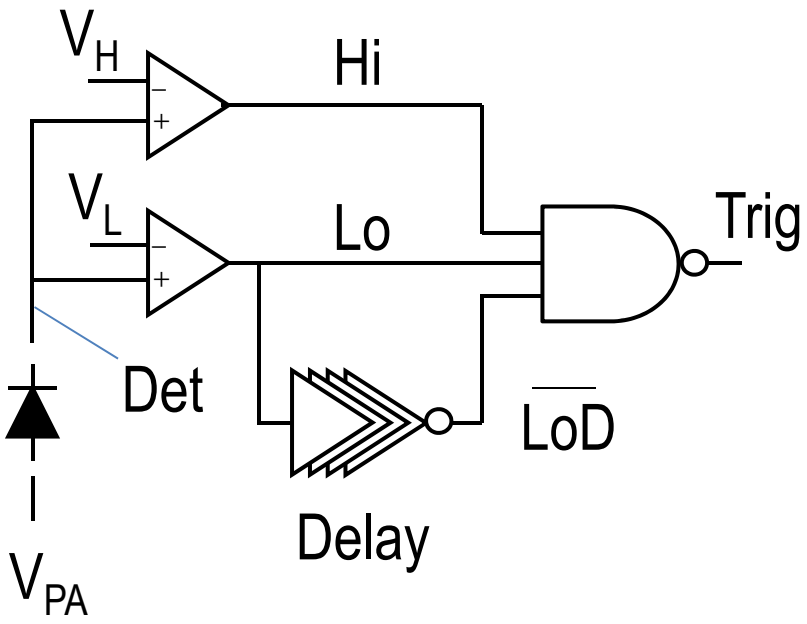
6 x 6 x 6 = 216 settings

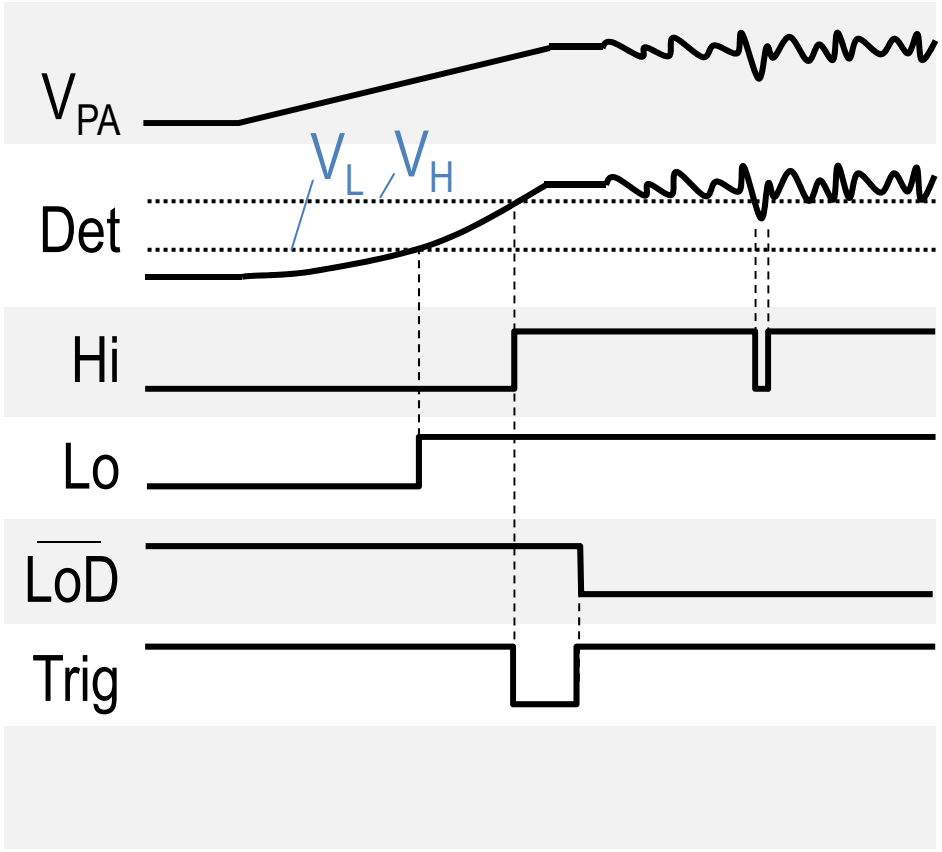
Detailed Block Diagram



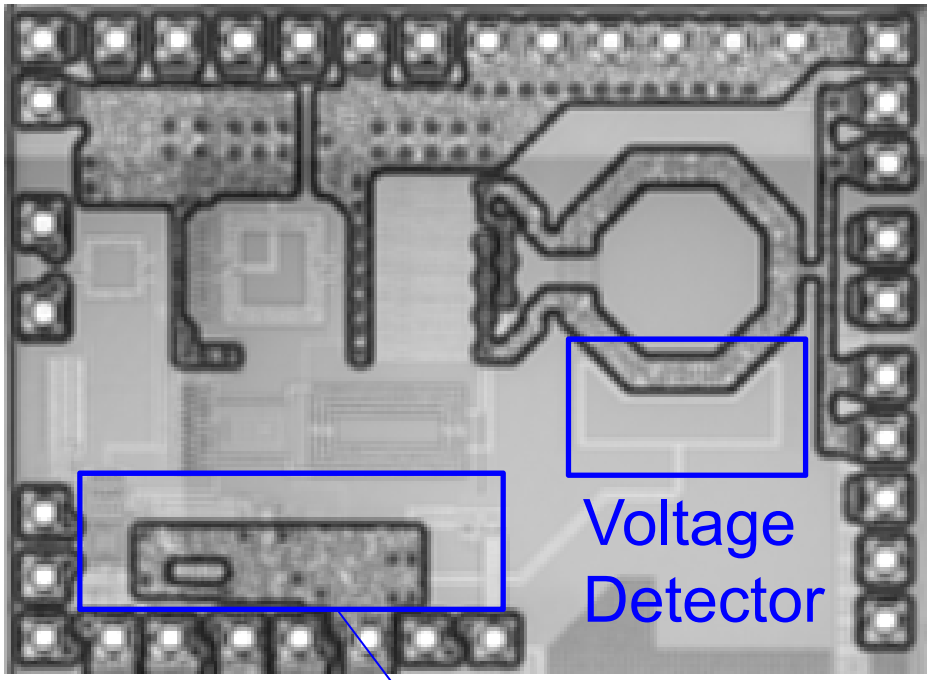
Burst Detector

- Prevent false detection with two reference levels





CMOS-PA Die Micrograph



- 130nm CMOS
- 1.6mm x 2.2mm
- 10μm thick top Cu by Plating

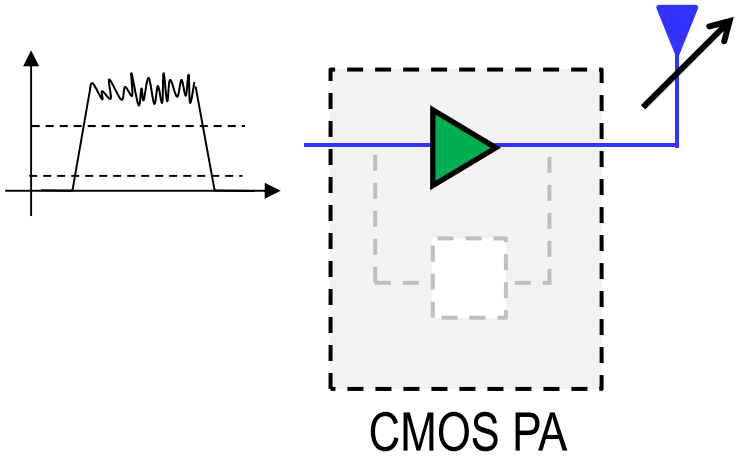
Reference Amplifier	Phase Detector
Zref	Envelope OTA
Attenuator	Burst Detector
	Quantizer

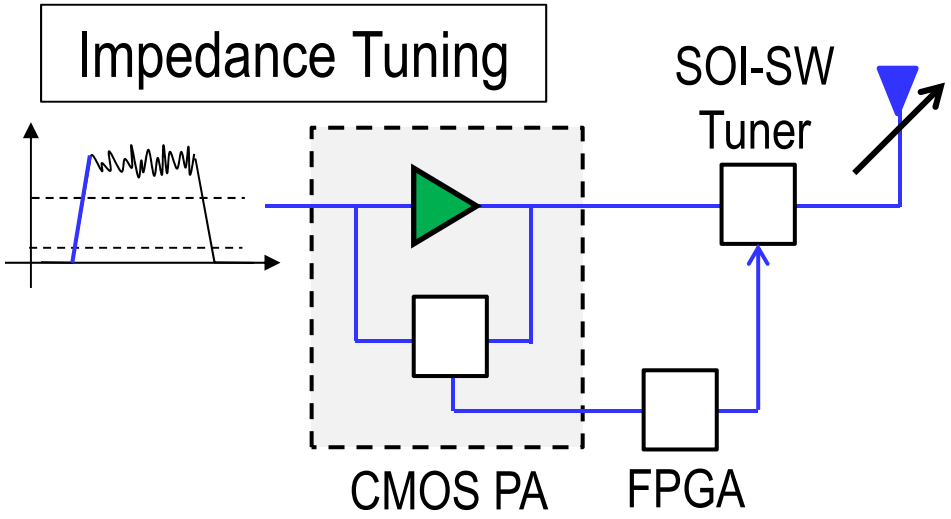
Measurement Setup

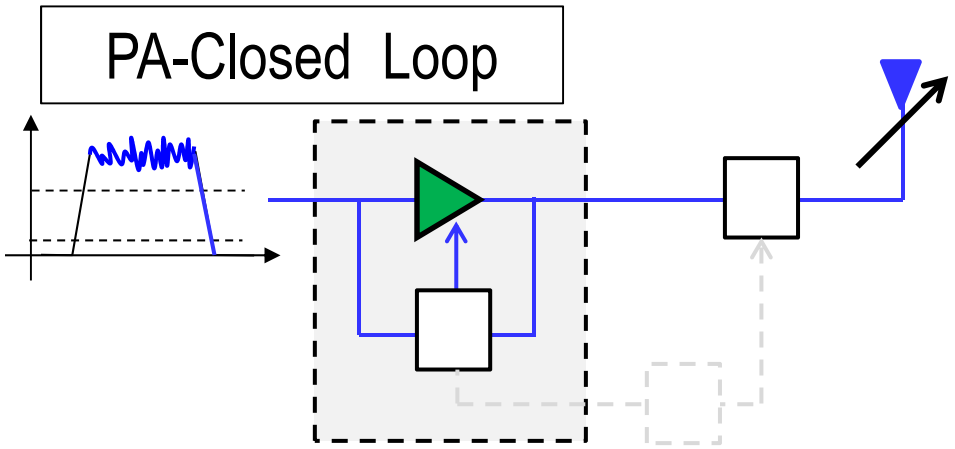
Off

On

1.95GHz
WCDMA
PAPR=3.5dB

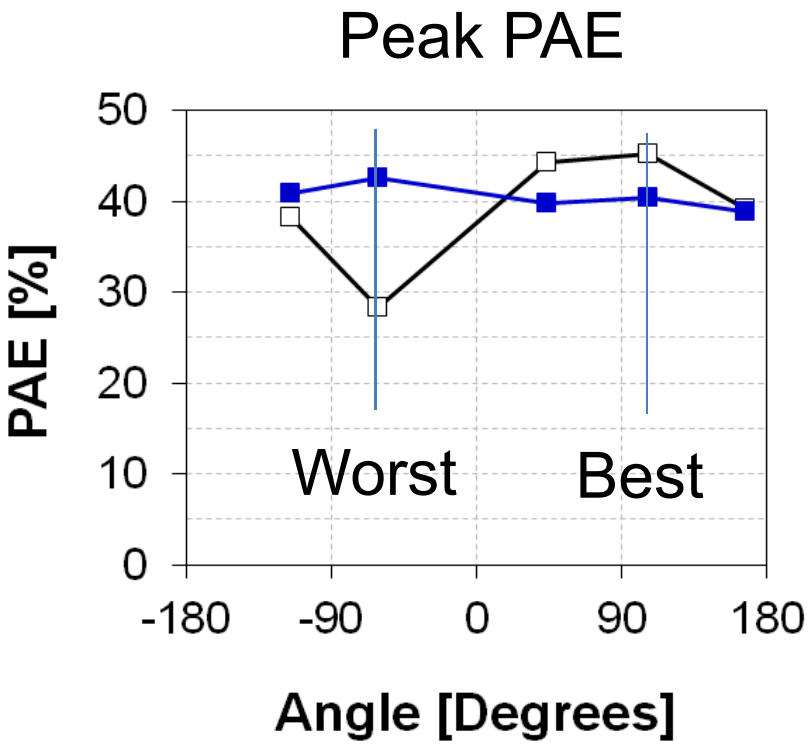


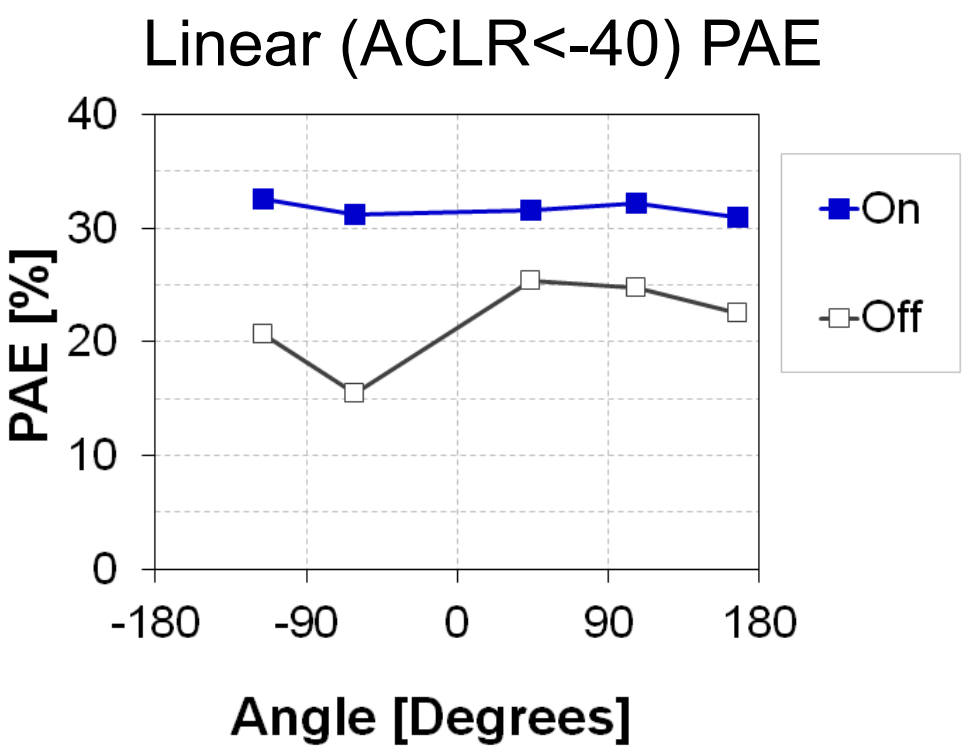




Antenna Impedance Dependency

- Constant PAE over load angle and improved linear PAE with PA-closed Loop and impedance tuning

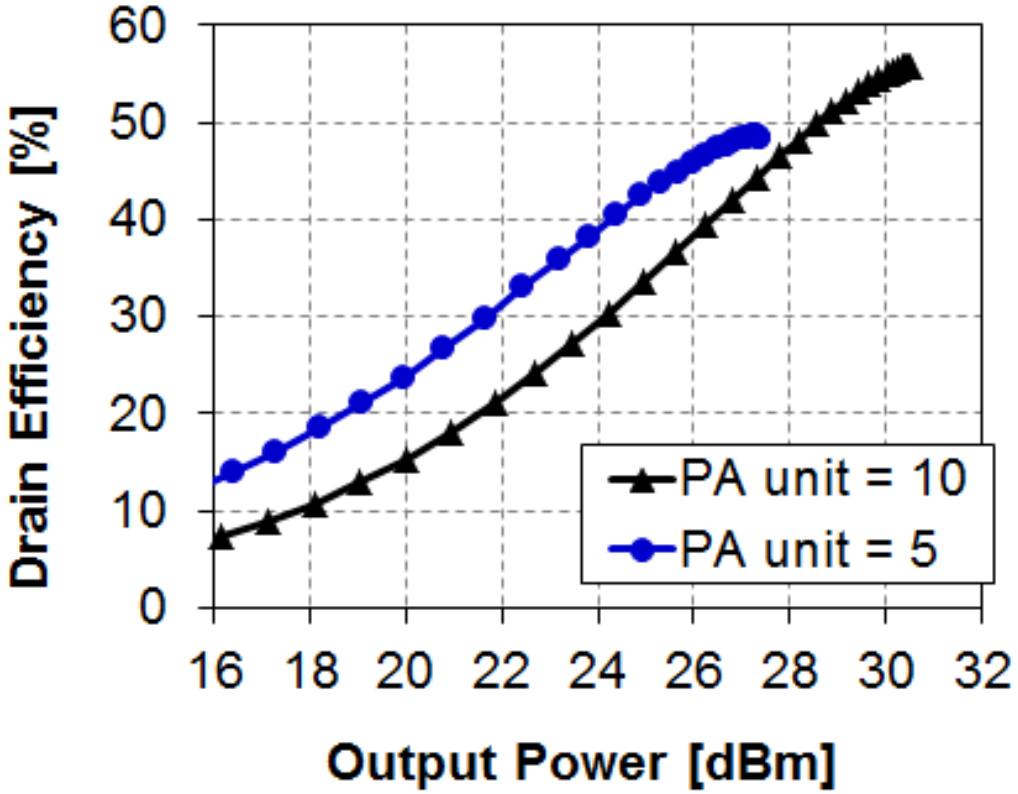




VSWR=2.5 *Tuner loss included

Back-off Efficiency

- Improved back-off efficiency with 5 PA units
- Impedance tuned to approximately 100Ω



*Tuner loss not included

Measured Performance Summary

PA chip	
Frequency	1.95 GHz
Peak Output Power	30.8 dBm
Peak PAE	47%
WCDMA*[1] Linear Output Power *[2]	27.9 dBm
WCDMA PAE @Linear	38 %
LTE *[3] Linear Output Power *[4]	25.5 dBm
LTE PAE @Linear	30 %
Tuning	
Impedance measurement accuracy	VSWR of 1.2
Tuner loss	0.3-1.6 dB

*1 PAPR is 3.5dB. *2 ACLR is 40dB.

*3 Bandwidth is 5MHz and 1% PAPR is 5.0dB. *4 ACLR is 35dB.

Performance Comparison

	ISSCC2009 [2]	This work
Detection target	Magnitude only	Polar
Optimization method	Exhaustive search	Successive approximation (Thermometer)
Required calibration steps	$O(N)$	$O(N^{0.5})$
Calibration time per step	1 μsec	8 μsec *1
Non-50Ω tuning	No	Yes
Time-varying input	No	Yes
Power consumption	27.5 mW	30 mW

*1 Limited by the burst detector

Conclusions

- Polar antenna tuning scheme is introduced to:
  - Improve efficiency,
  - Ease the RF front-end implementation, and
  - Without increasing BoM and cost.

- Proposed tuning scheme is implemented on a CMOS PA chip and its effectiveness is verified with the prototype of SOI-SW-based impedance tuner.
  - VSWR dependency
  - Back-off efficiency improvement

Acknowledgement

- Authors would like to thank for Dr. Hua Wang from Georgia tech for discussions and suggestions.

- Authors would like to thank for Mr. Junji Wadatsumi and Discrete division of Toshiba.

3.2
A 1.95GHz Fully Integrated Envelope Elimination and Restoration CMOS Power Amplifier with Envelope/Phase Generator and Timing Aligner for WCDMA and LTE

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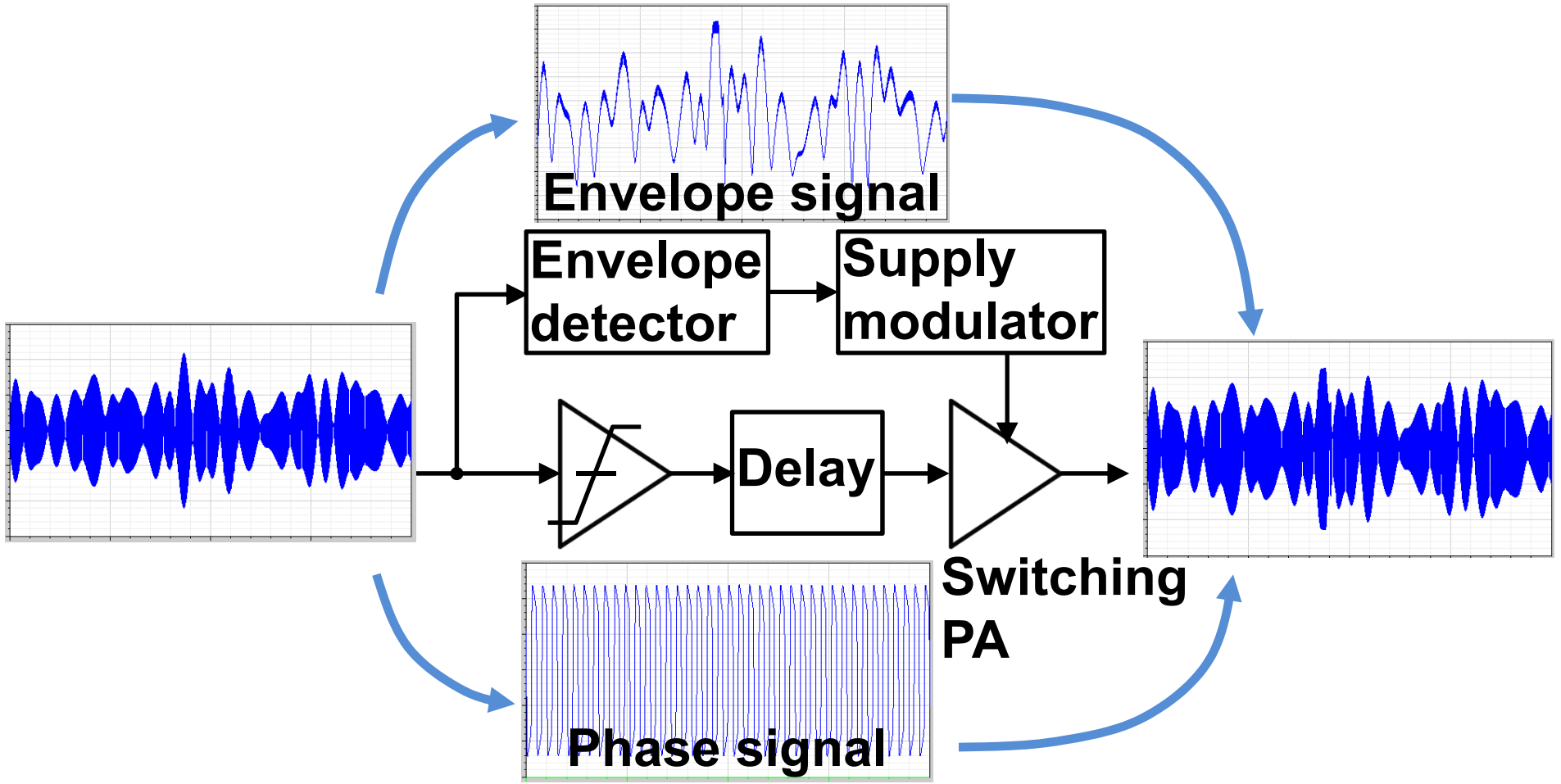
1 Fujitsu Laboratories LTD, Japan
2 Fujitsu Semiconductor LTD, Japan

Outline

- Introduction
  - Background for envelope elimination and restoration (EER)
  - Efficiency improvement
  - Challenges to low distortion
- Implementation
  - Envelope and phase signals generation
  - Timing alignment
- Measurement results
- Conclusion

Envelope elimination and restoration (EER)

- Separation of envelope and phase signals
- Restoration of modulated RF signal at switching PA



[L. Kahn, Proc. IRE, 1952]

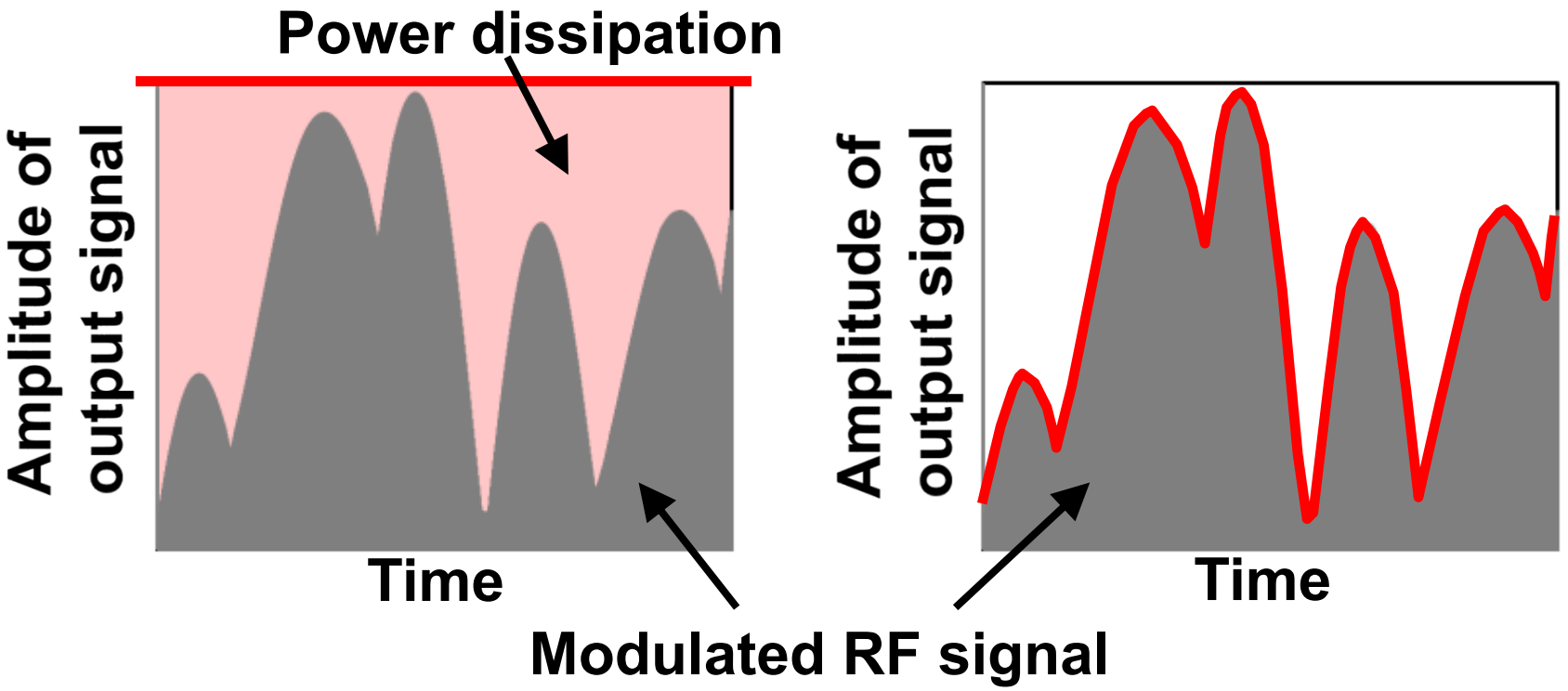
Efficiency improvement

- **By using supply modulation**
  instead of conventional fixed supply voltage

- **By using switching PA**
  instead of conventional linear PA with fixed supply or envelope tracking (ET)

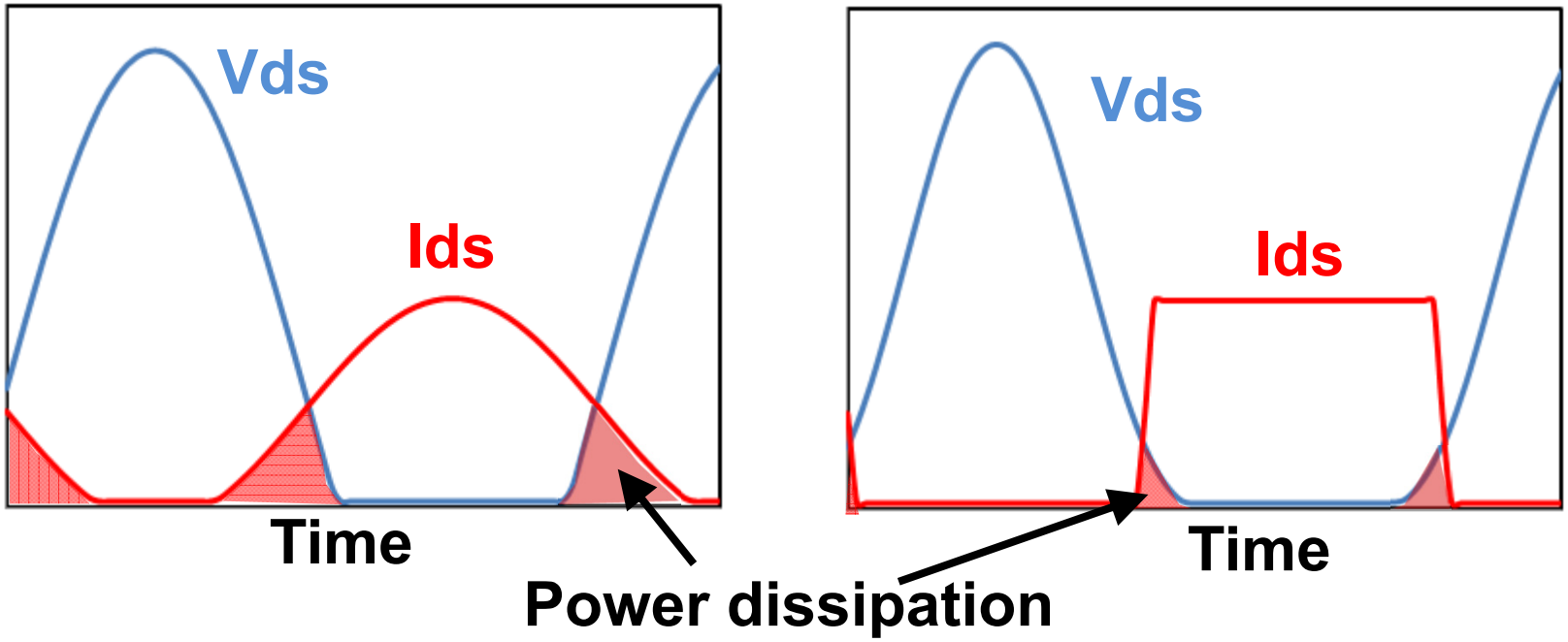
High efficiency by supply modulation

- Small power dissipation by reducing excessive supply voltage



High efficiency by switching PA

- Small power dissipation at transistor



(a) Linear PA (Conventional)

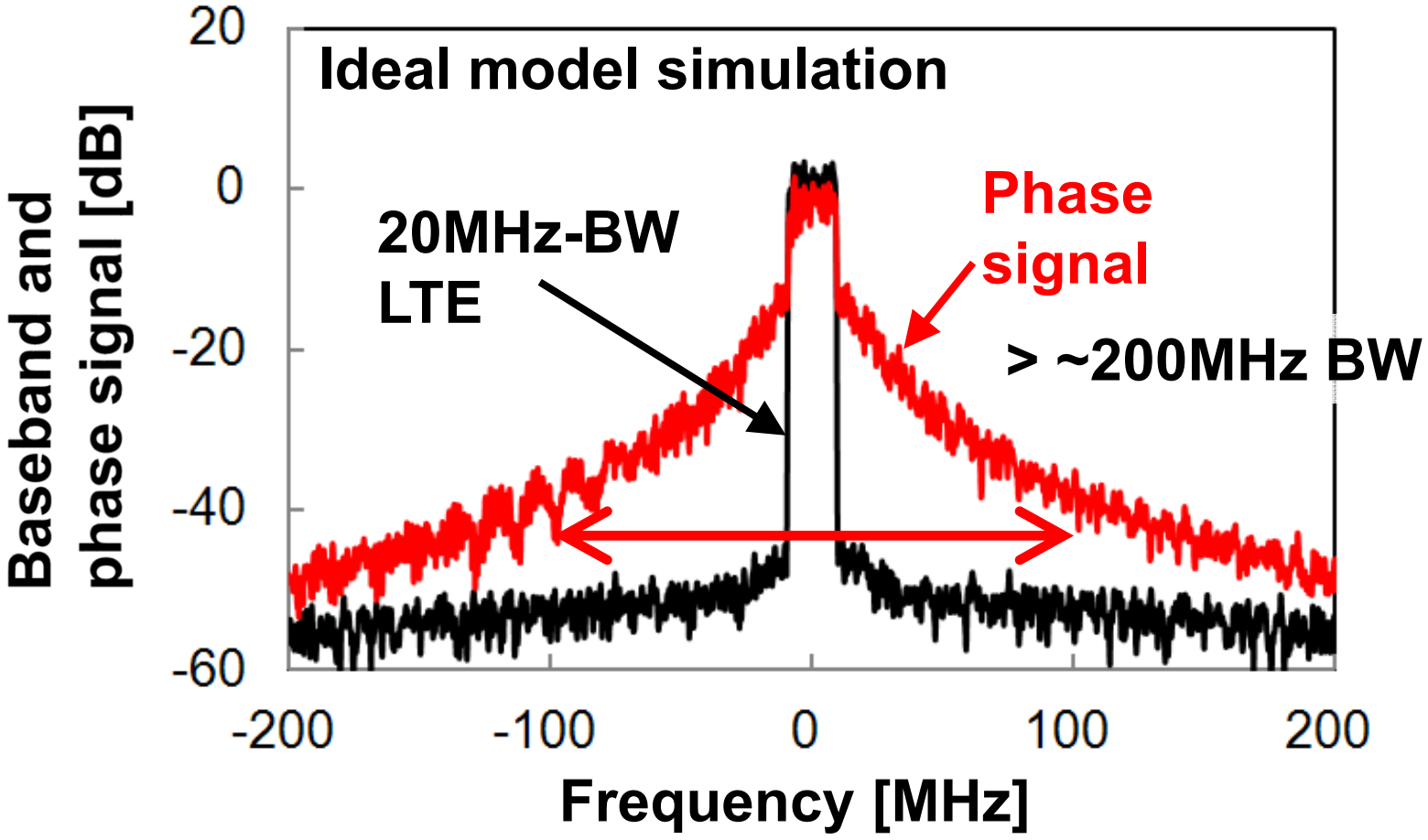
(b) Switching PA (EER)

Challenges in EER design for LTE

- **Challenge 1: Wide BW phase signal (>~200MHz)**
- **Challenge 2: Small timing mismatch between envelope and phase signals (< 1ns)**

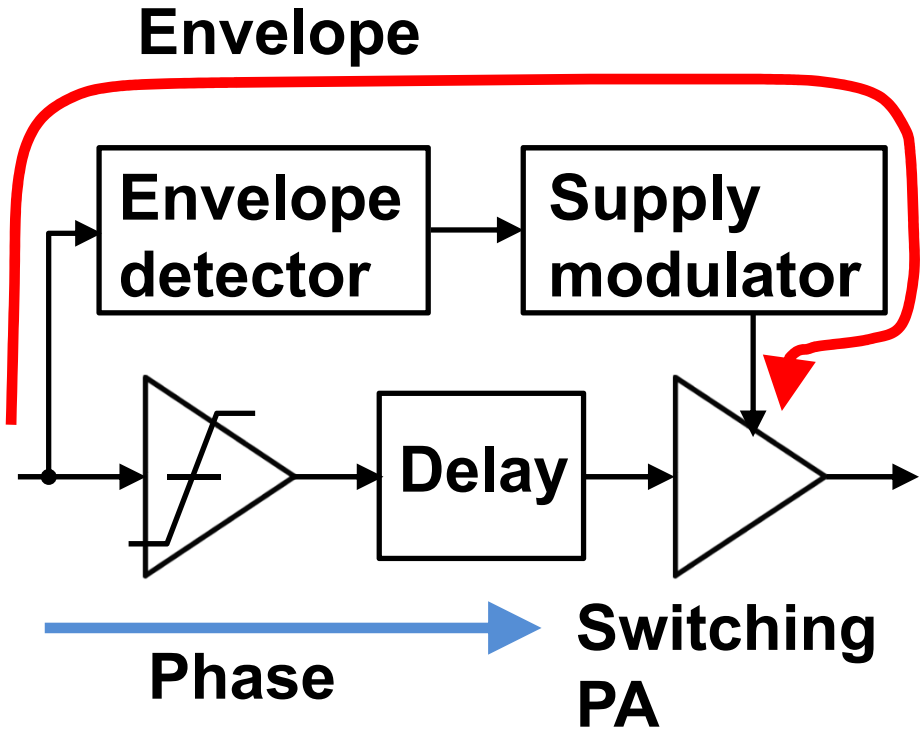
Challenge 1: Wide BW phase signal

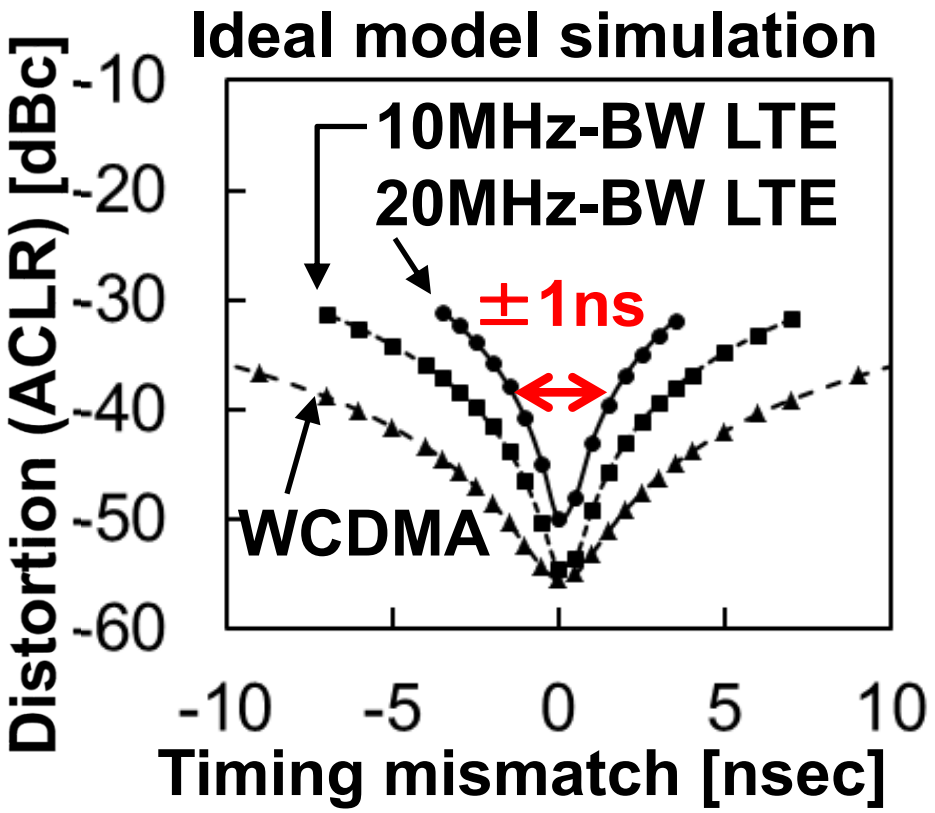
- > ~200MHz BW required for phase path
- Distortion deteriorated by narrow BW circuits



Challenge 2: Small timing mismatch

- Distortion deteriorated by timing mismatch between envelope and phase signals
- < 1ns timing mismatch required for 20MHz-BW LTE



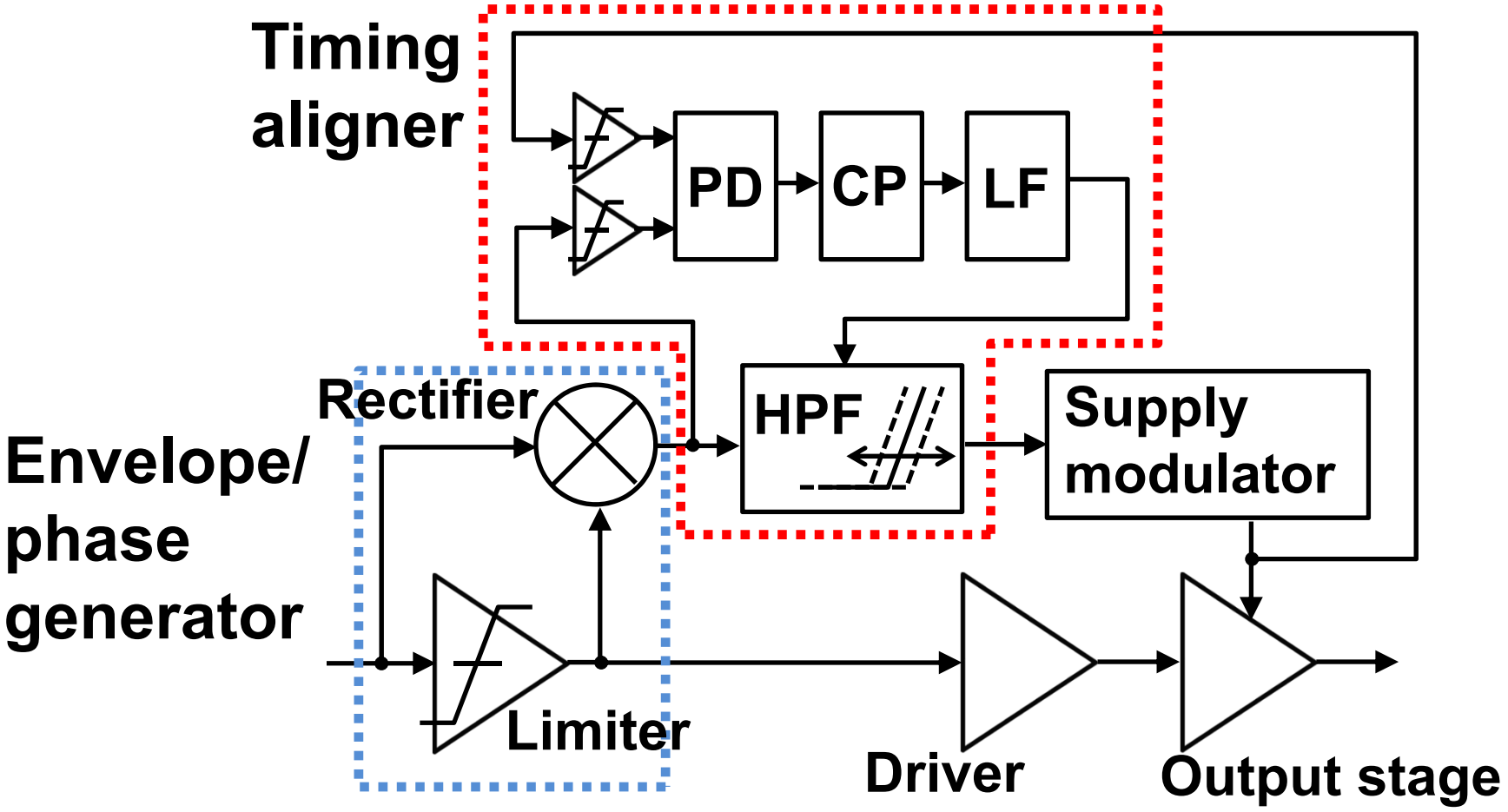


Outline

- Introduction
  - Background for envelope elimination and restoration (EER)
  - Efficiency improvement
  - Challenges to low distortion
- Implementation
  - Envelope and phase signals generation
  - Timing alignment
- Measurement results
- Conclusion

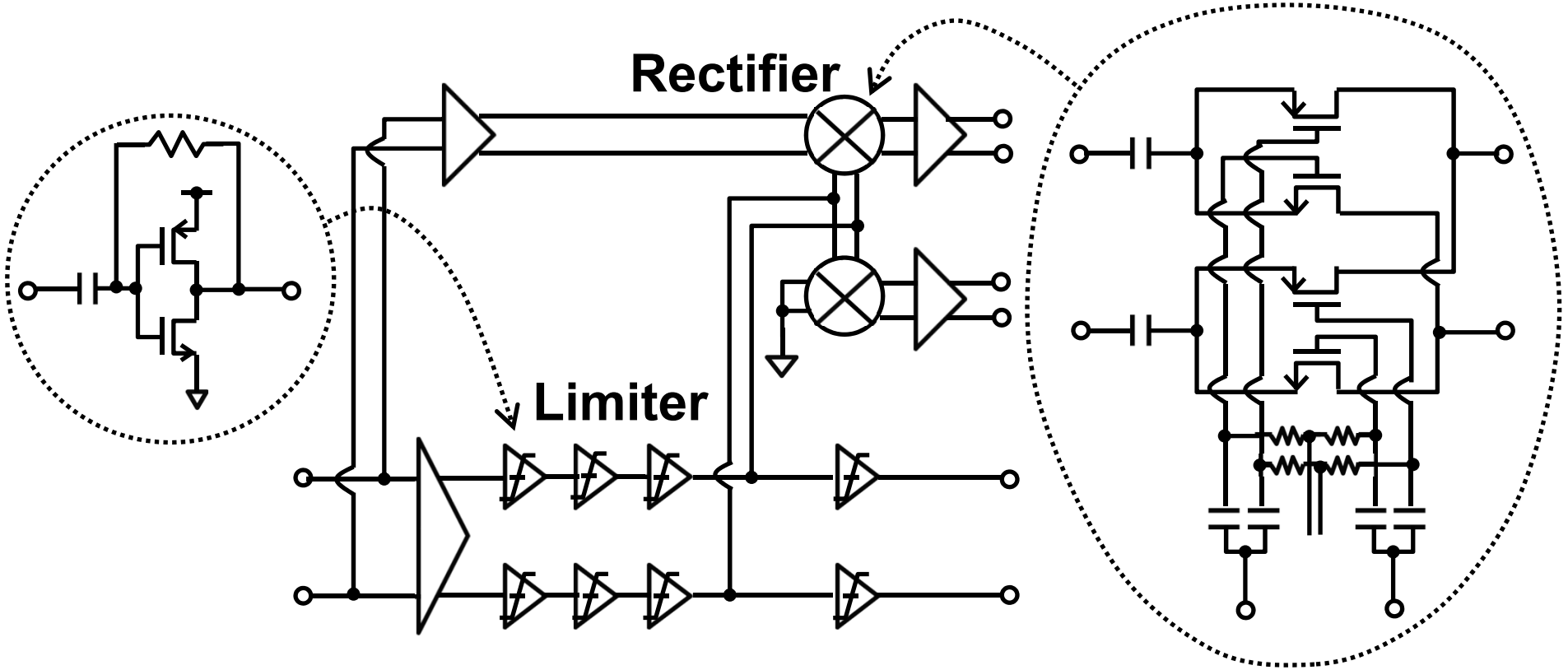
Overview of our solution

- Wide BW phase path in envelope / phase generator
- Small timing mismatch by timing aligner based on DLL



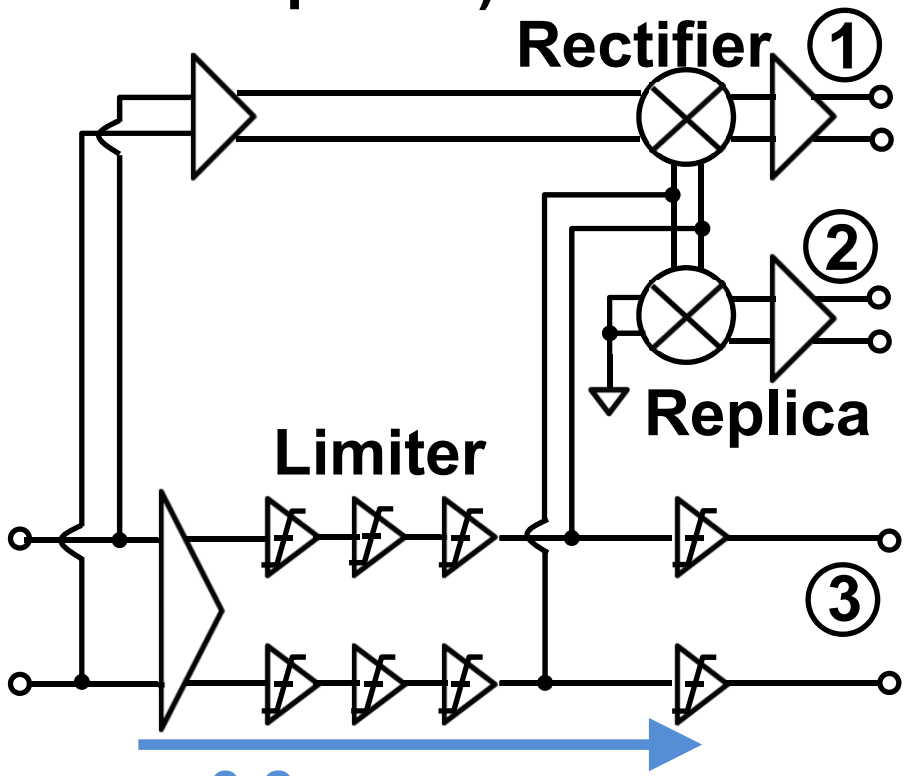
Envelope / phase generator (Challenge 1&2)

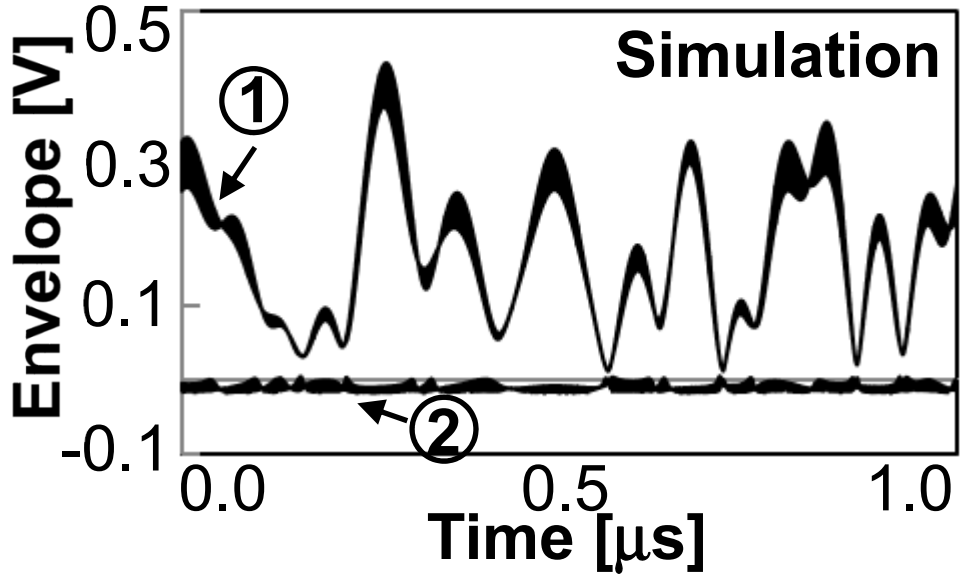
- Wide BW and small delay phase signal
  (Limiter based on CMOS inverter)
- Low distortion envelope signal
  (Full-wave rectifier based on passive MIX)

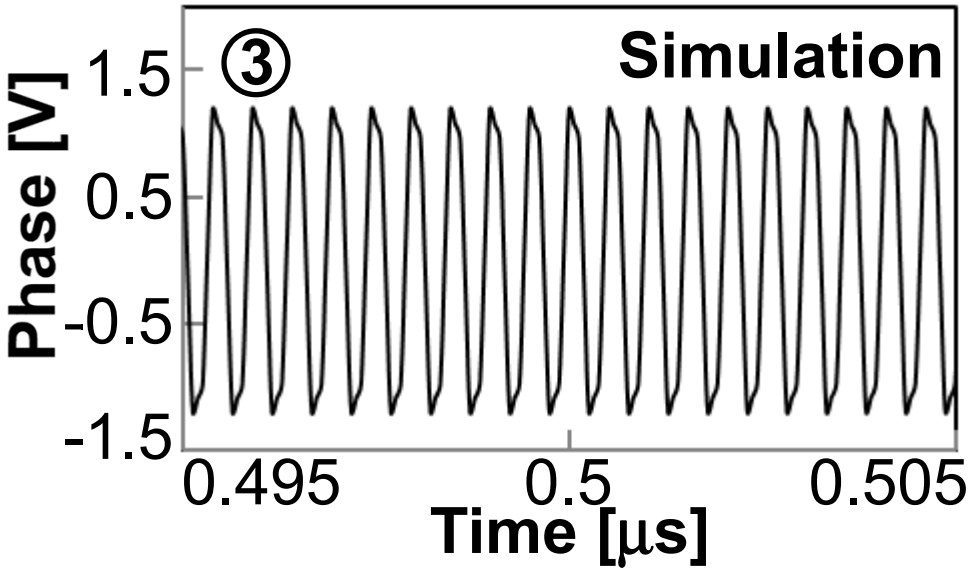


Envelope / phase generator (Challenge 1&2)

- < 0.3ns simulated phase path delay (< 1ns mismatch required)

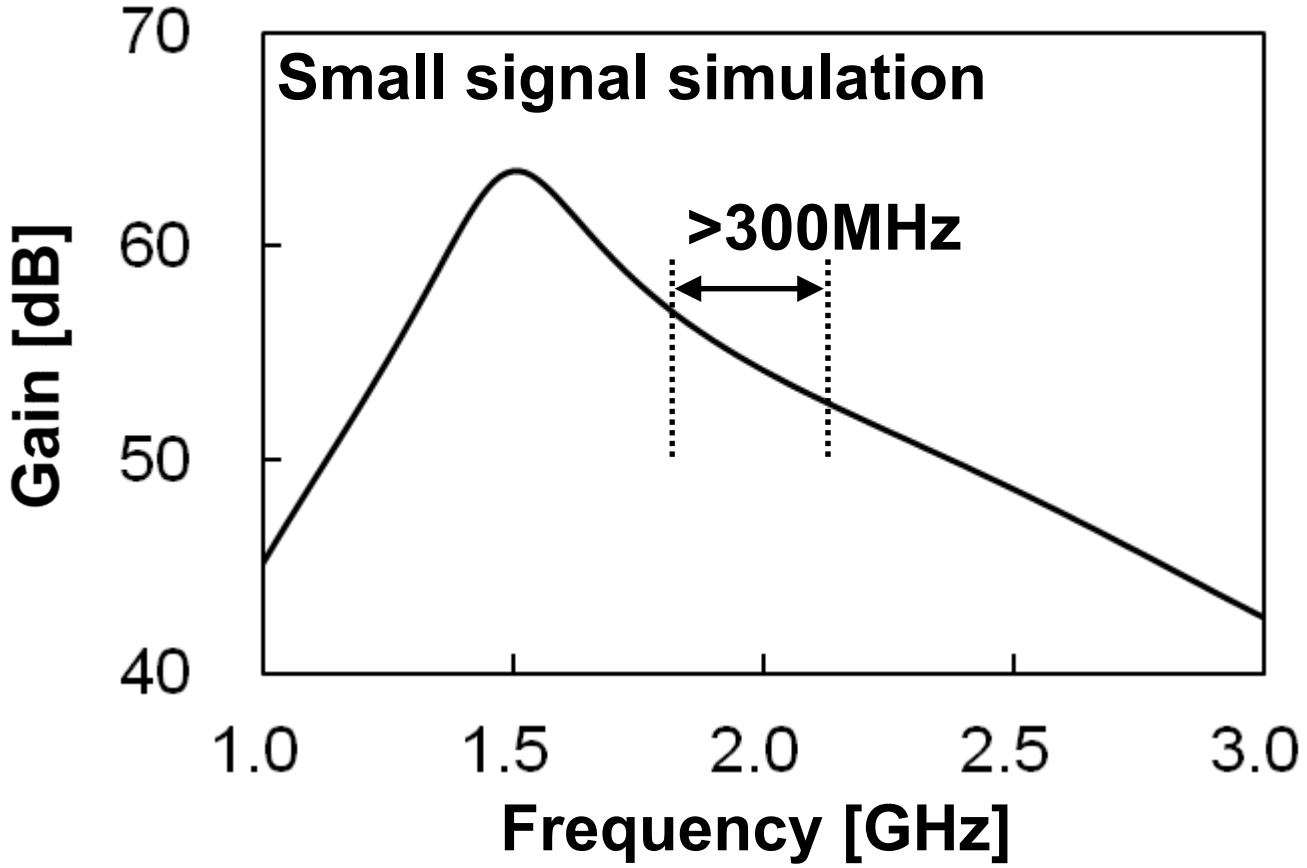






Wide BW phase path

- > 300MHz BW within ±3dB gain deviation
  (> ~200MHz-BW required)

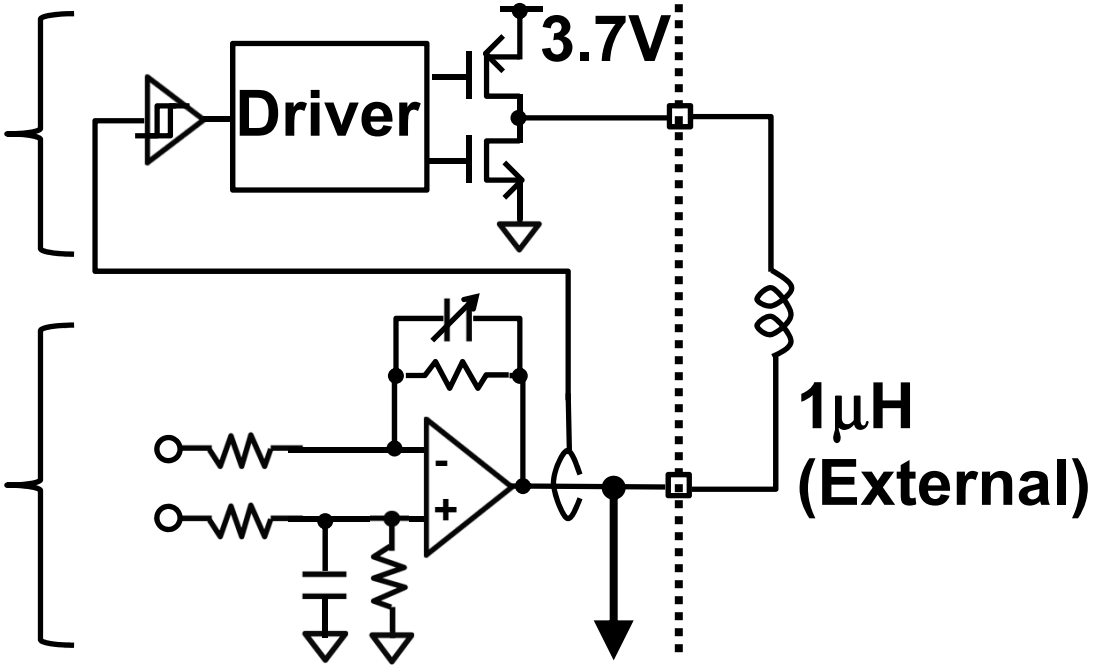


Supply modulator

- Both high efficiency and high speed are achieved

Switching regulator
- High efficiency
- Low speed

Linear regulator
- High speed
- Low efficiency

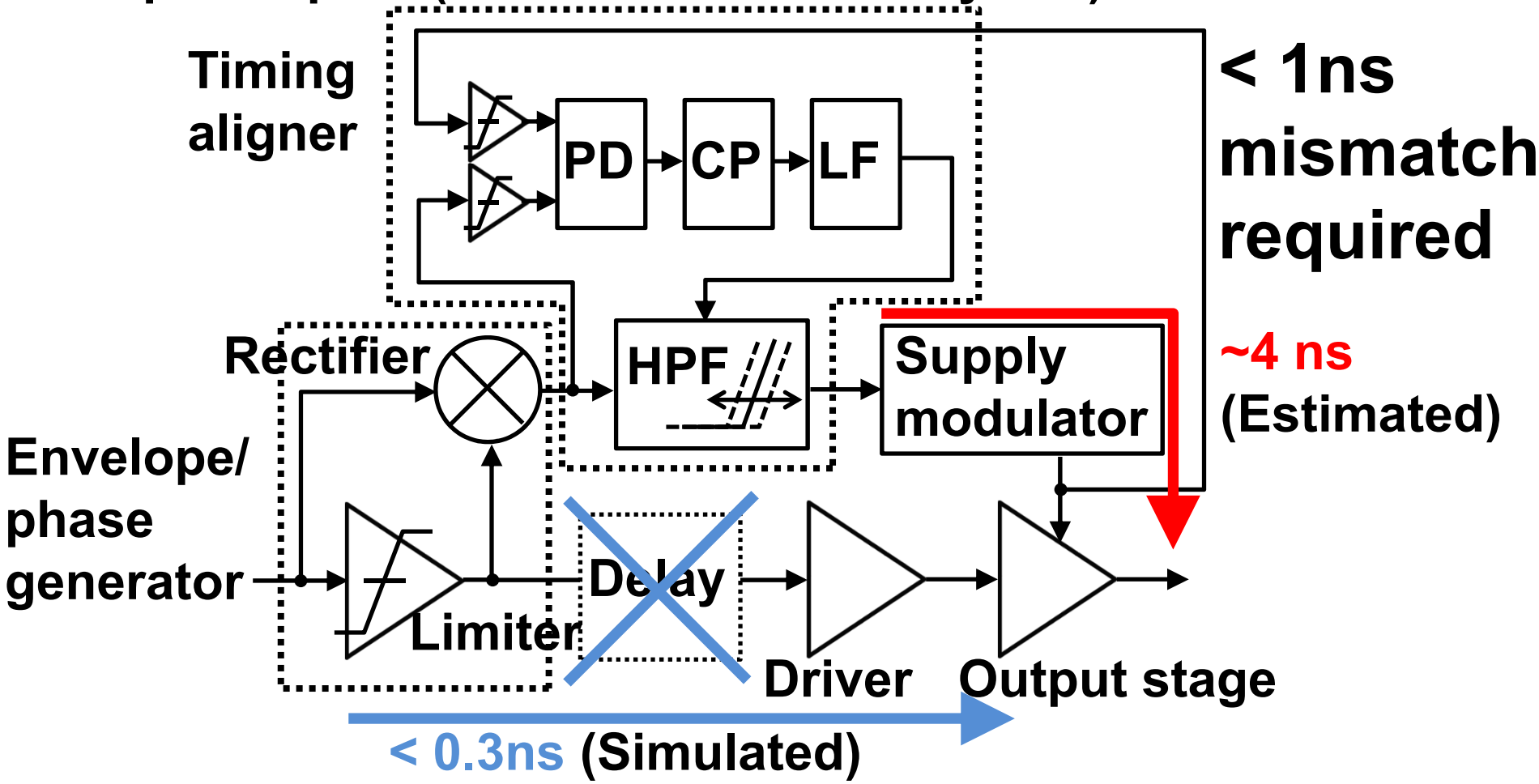


[F. Wang et al., IEEE Trans. Microw. Theory Tech., 2006]

	WCDMA	20MHz-BW LTE
Cut-off frequency	~10MHz	~40MHz
Estimated delay	~16ns	~4ns
Simulated efficiency	~80%	~70%

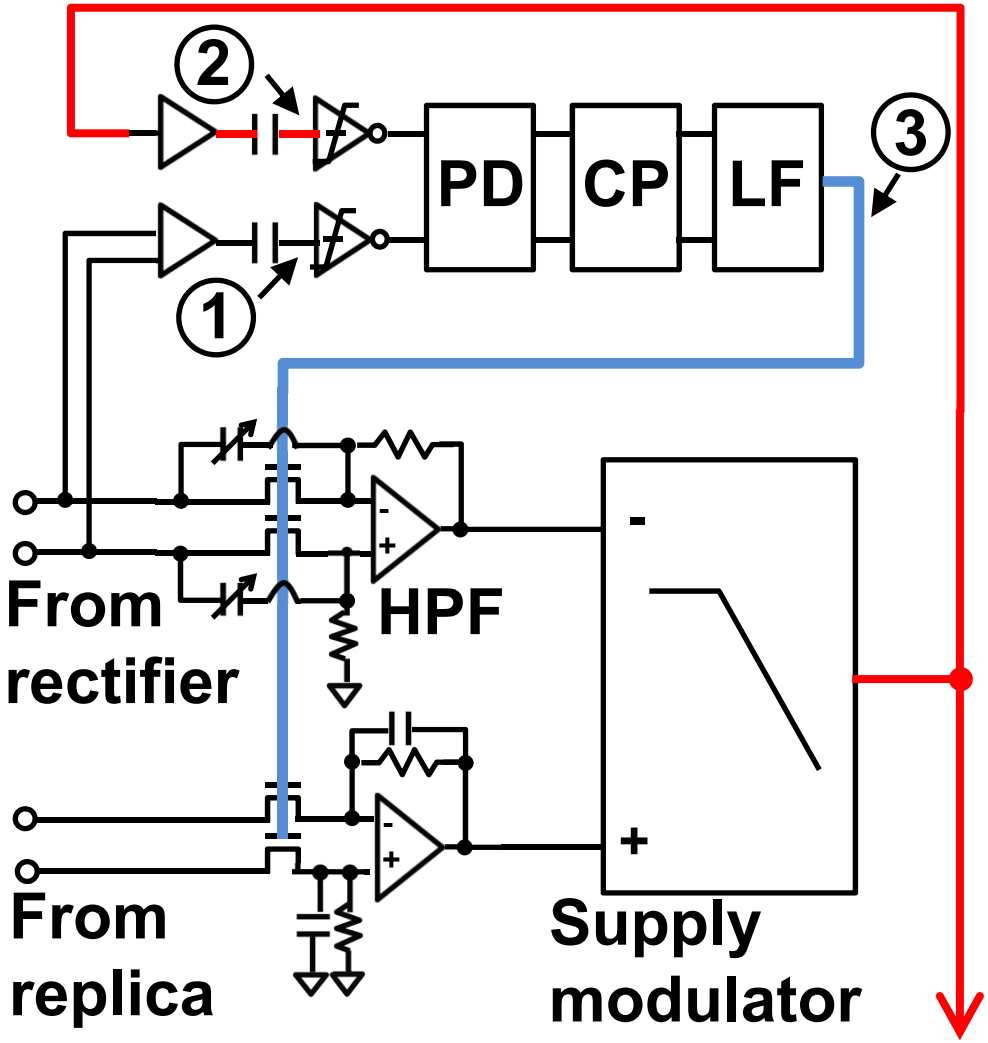
Envelope and phase delays analysis

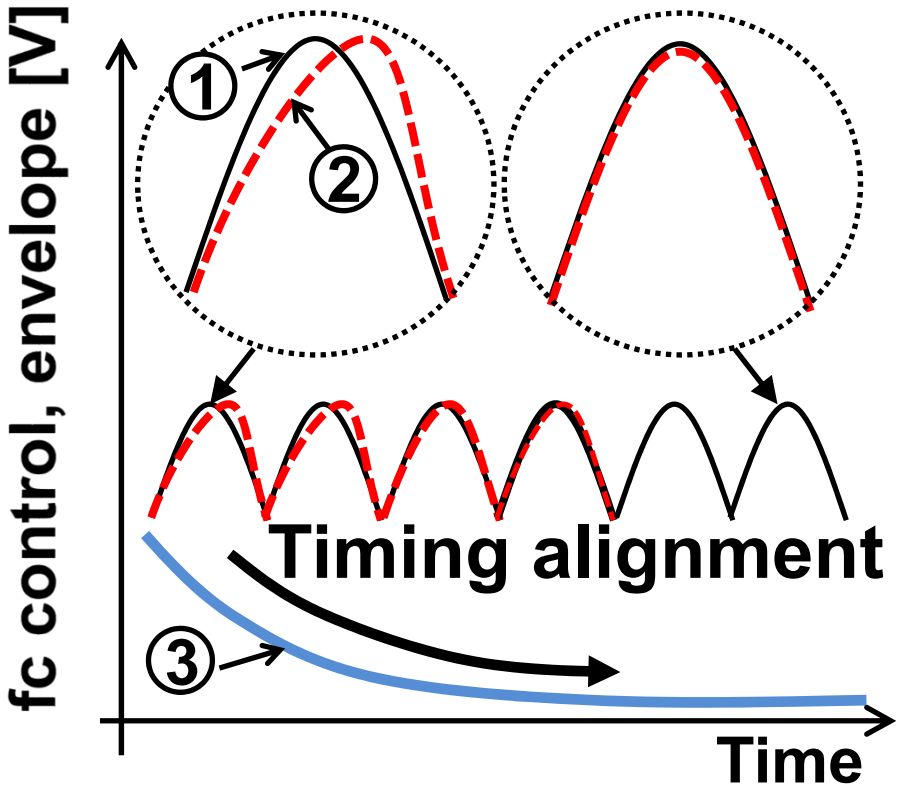
- Timing mismatch generated by envelope path
- Timing alignment by HPF instead of additional delay in phase path (troublesome ~8 RF cycles)



Timing aligner (Challenge 2)

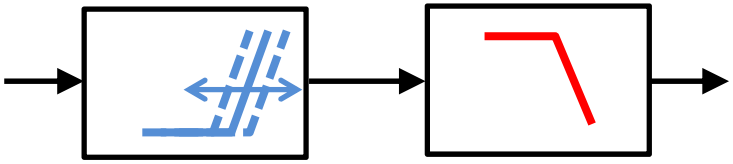
- DLL compensates for positive delay of supply modulator by adjusting negative delay of variable HPF





BW expansion by timing aligner

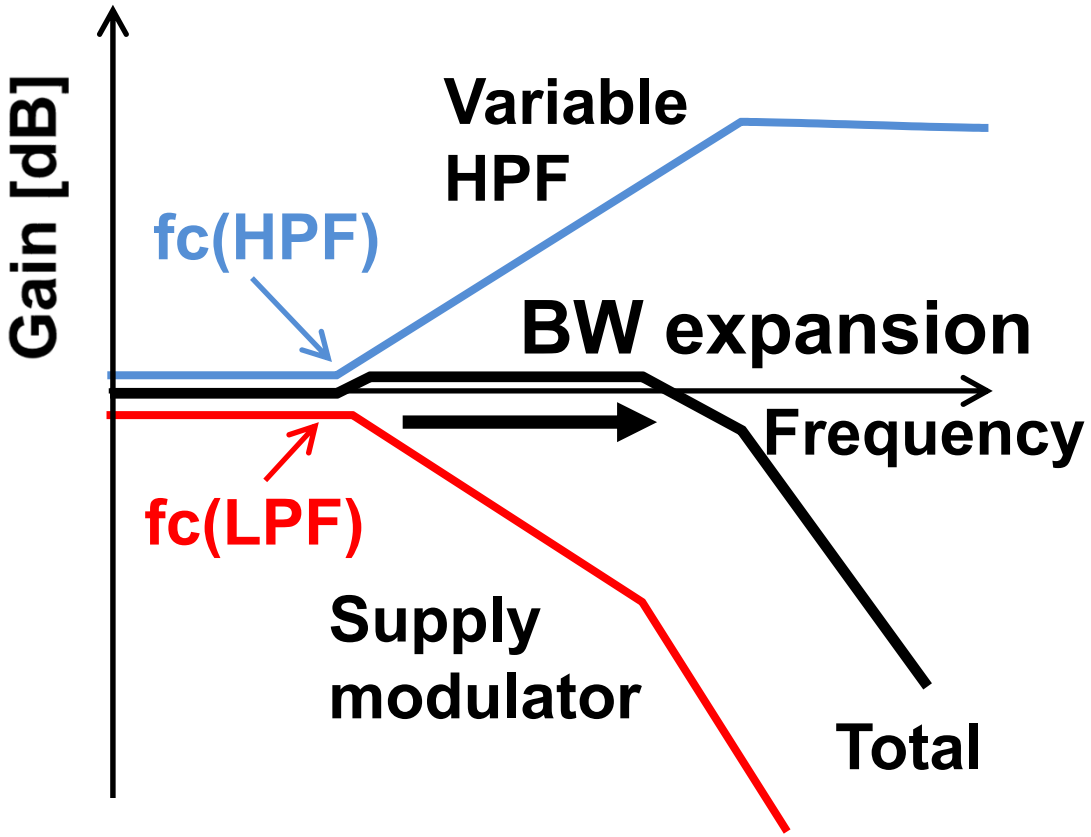
- Total transfer function flattened by variable HPF before supply modulator (LPF)



$$A_1(1+sR_1C_1) \times \frac{A_2}{(1+sR_2C_2)}$$

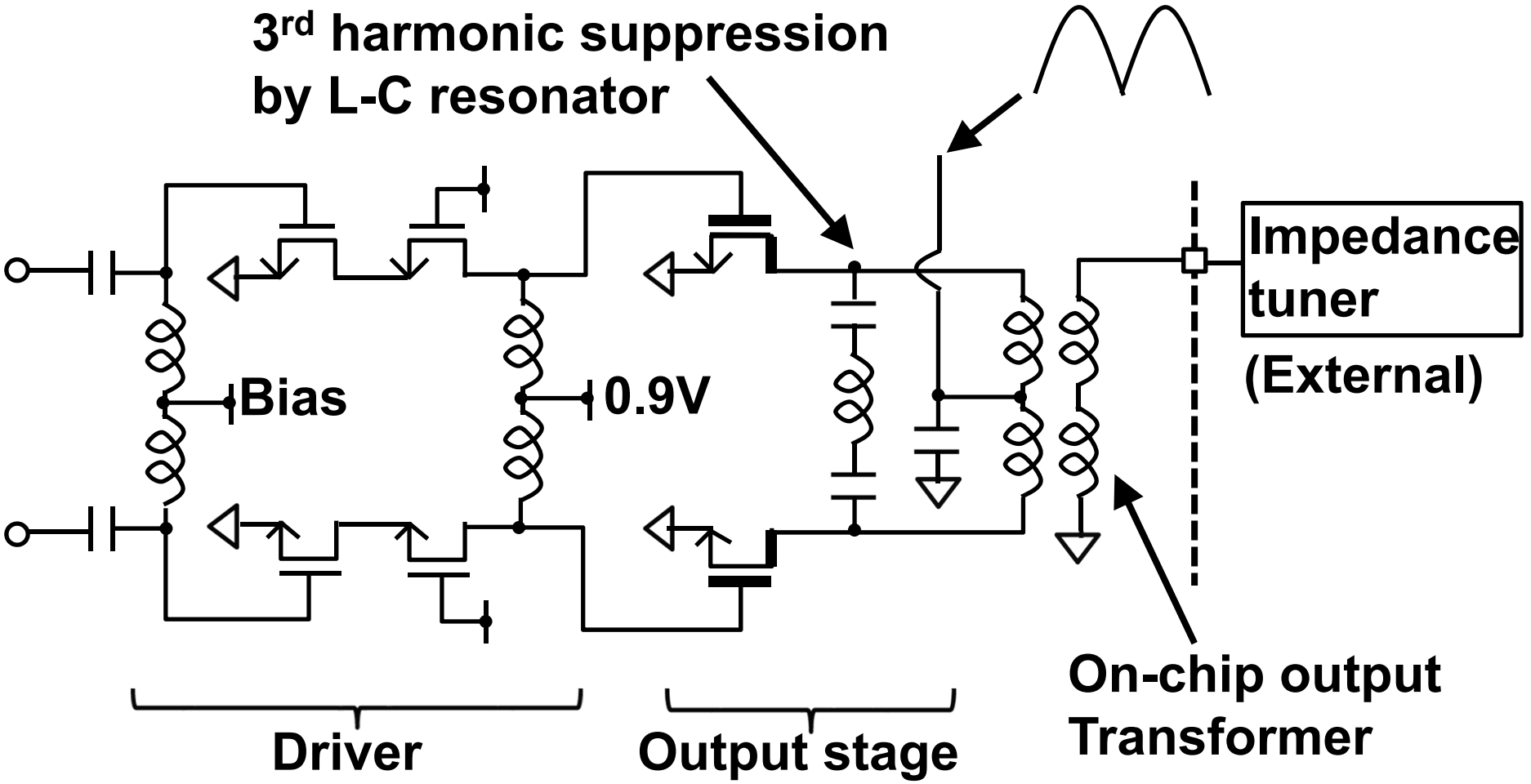
$$= A_1A_2$$

when $R_1C_1=R_2C_2$



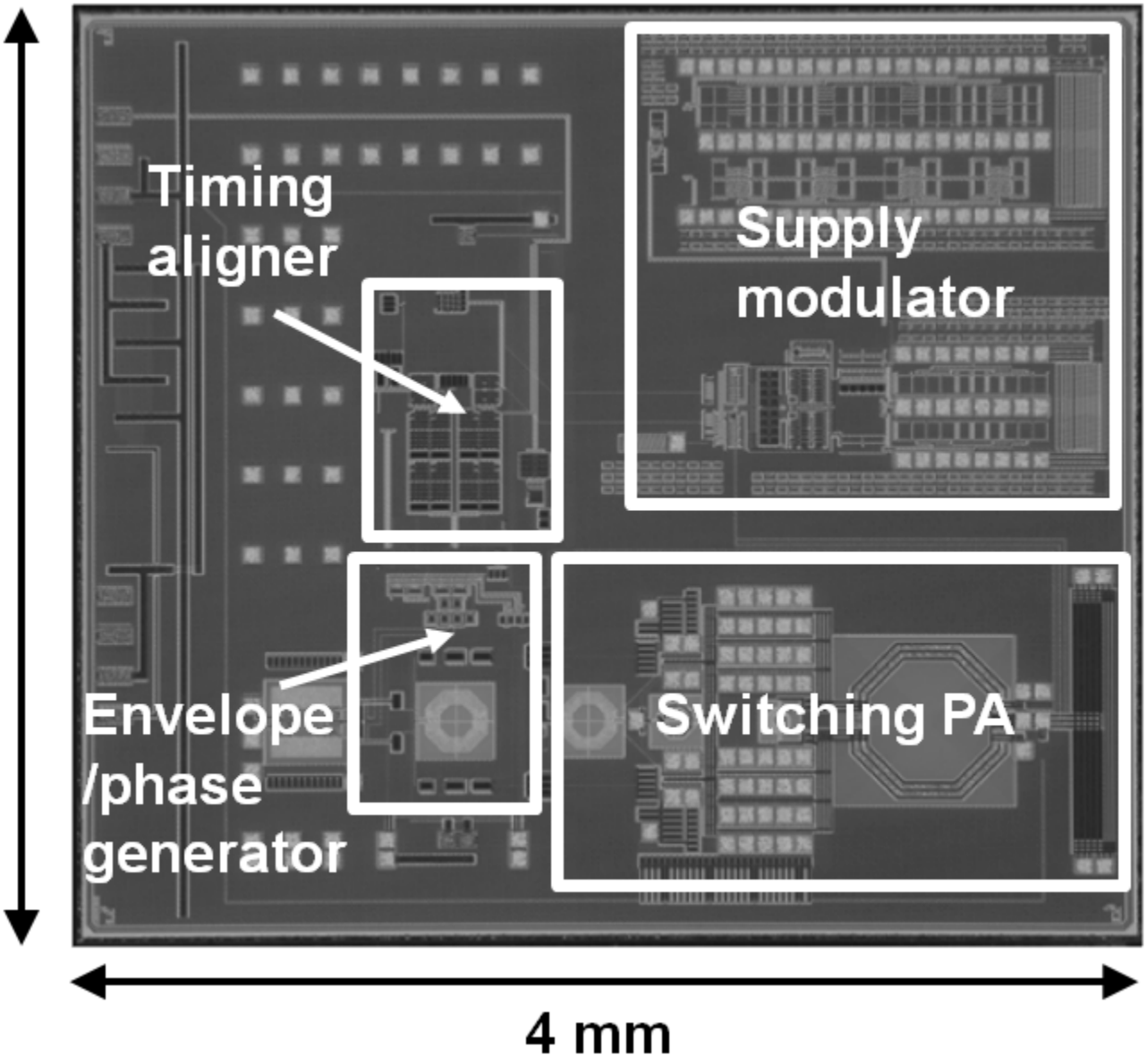
Switching PA

- 2 stage amplifier composed of 90nm MOS and high breakdown voltage transistors



Micrograph of the test chip

90nm CMOS with 3μm-thick metal option



Outline

- Introduction
  - Background for envelope elimination and restoration (EER)
  - Efficiency improvement
  - Challenges to low distortion
- Implementation
  - Envelope and phase signals generation
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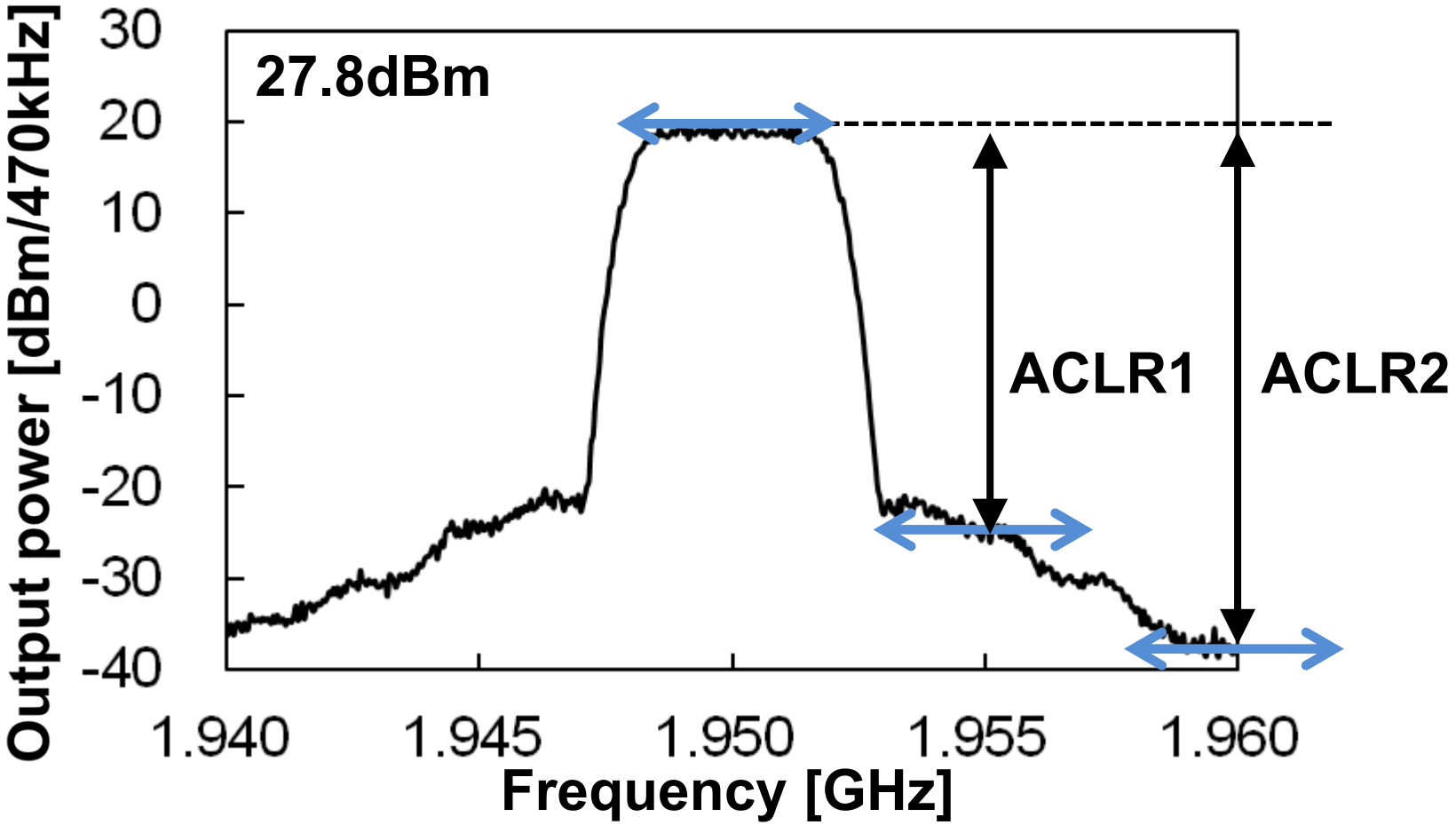
- Conclusion

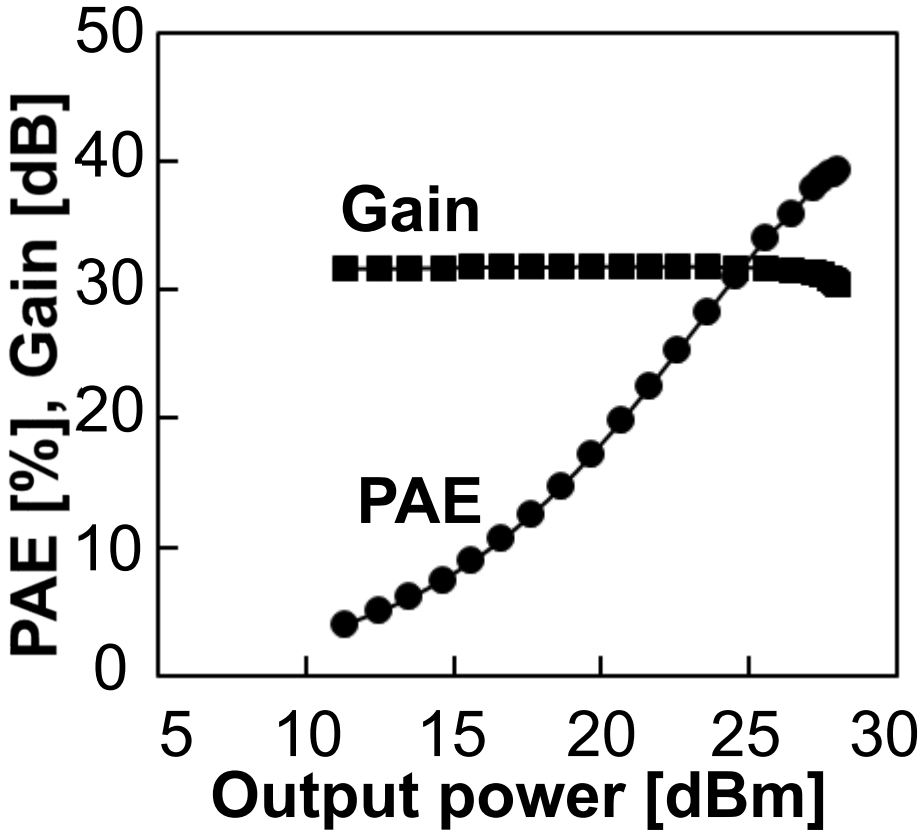
Output spectrum

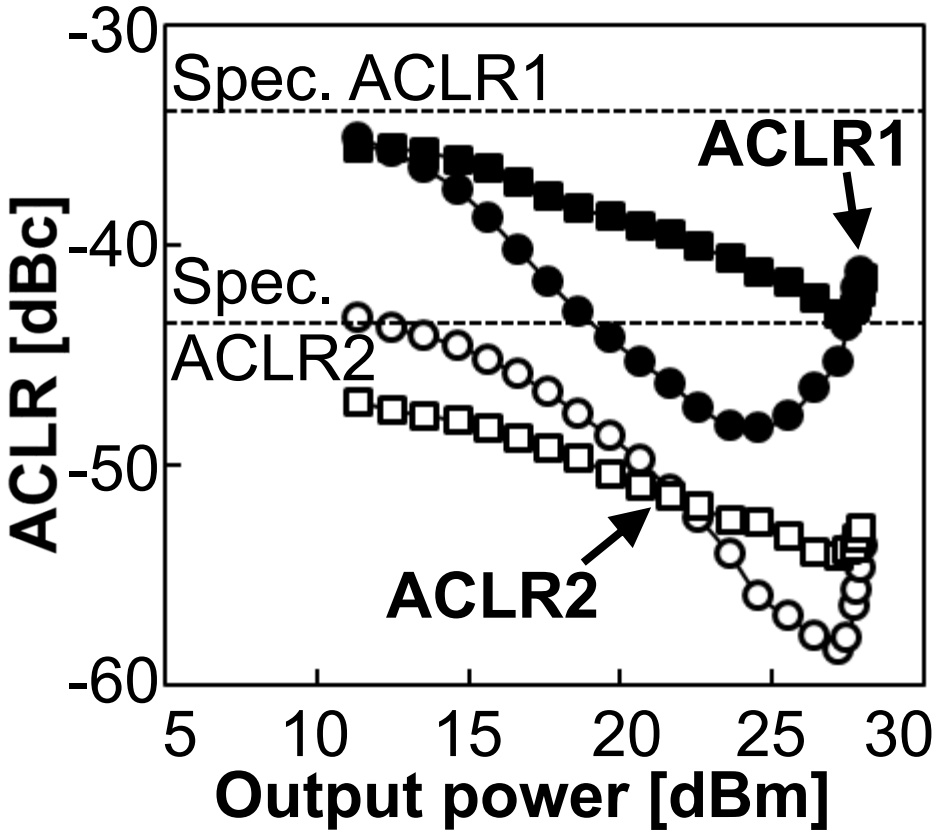
- WCDMA uplink
- Adjacent channel leakage ratio (ACLR) deteriorated by distortion



PAE and ACLR for WCDMA uplink

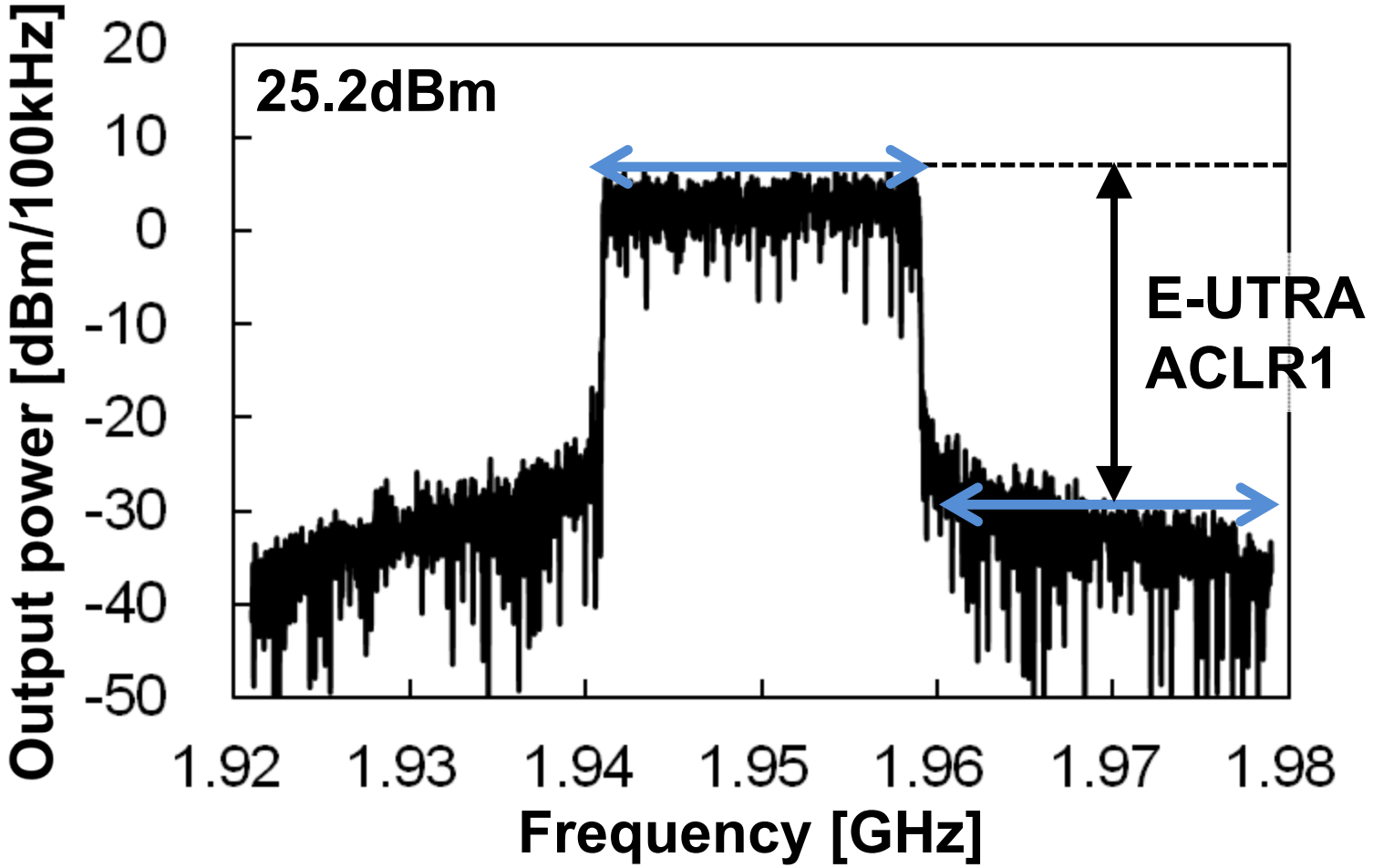
- **PAE = 39.2% and ACLR1 = - 41.1dBc at 28dBm**
  (PAE: Power-added efficiency)





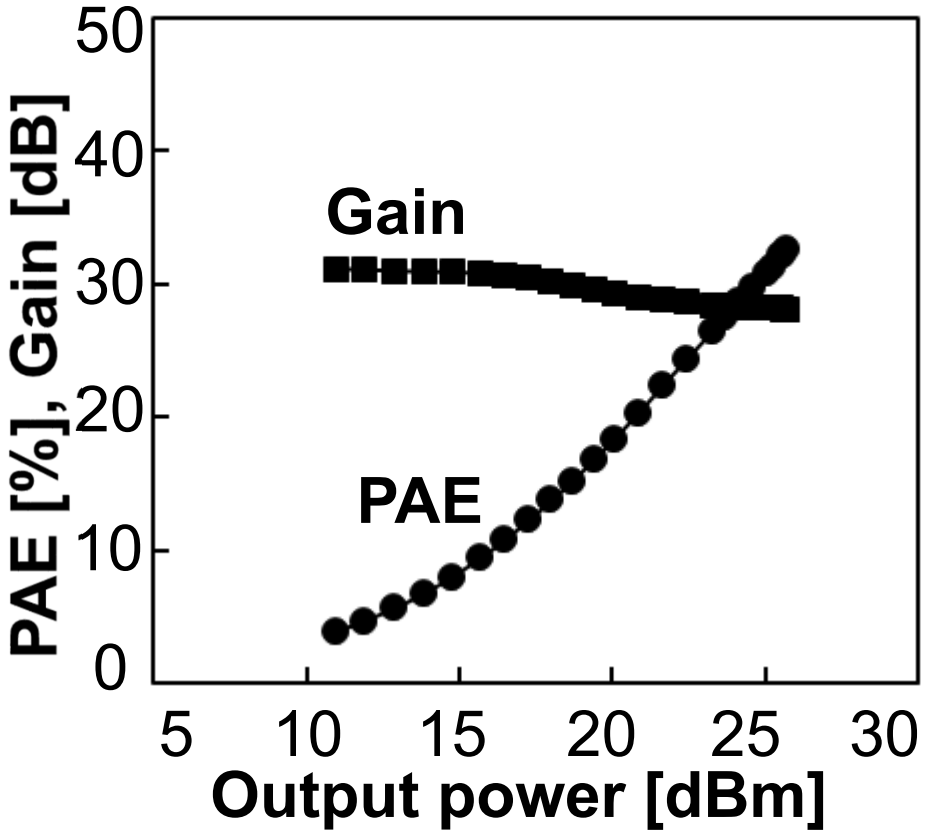
Output spectrum

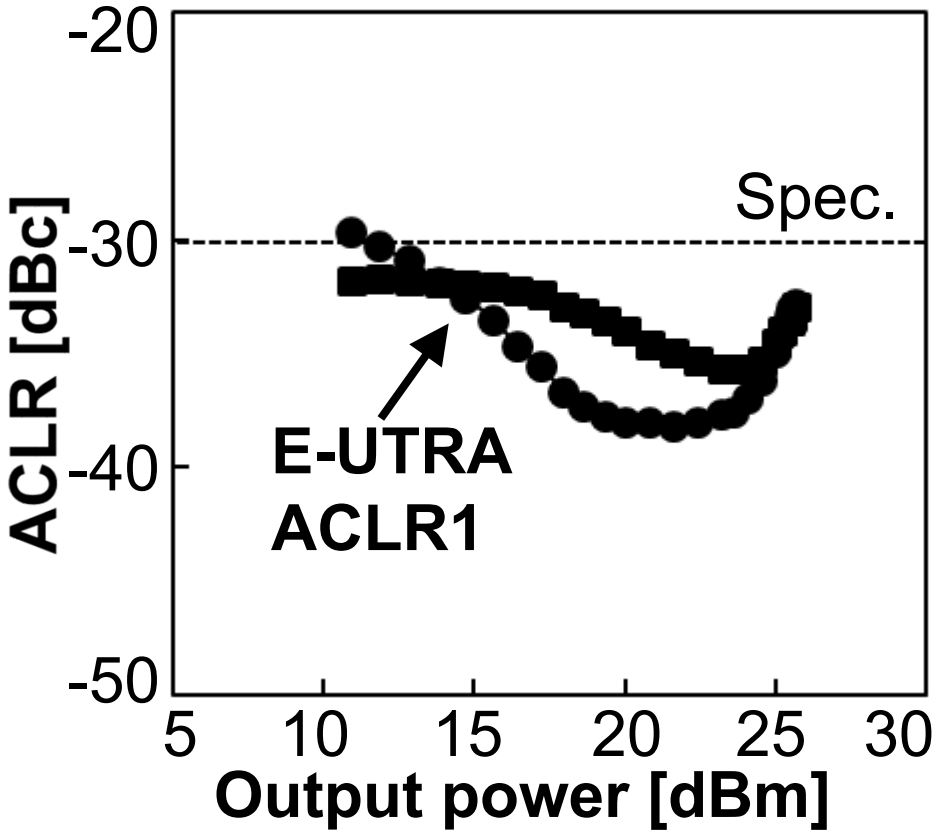
- 20MHz-BW 16QAM LTE uplink



PAE and ACLR for 20MHz-BW LTE uplink

- PAE = 32.2% and ACLR = - 33dBc at 25.6dBm





Performance comparison (WCDMA CMOS PAs)

	ISSCC'12 B. Koo et al.	ISSCC'12 K. Kanda et al.	ISSCC'12 S. Kousai et al.	**This work**
Frequency [GHz]	1.95	2	1.88	**1.95**
Output power [dBm]	28	27.4	27.1	**28**
Gain [dB]	23.7	27.3	28.3	**30.5**
PAE [%]	36.4	28.5	28	**39.2**
ACLR1 [dBc]	-35	-34	-40	**-41.1**
ACLR2 [dBc]	-	-	-52.1	**-52.8**
Output transformer	on-chip	on-chip	on-chip	**on-chip**
Technology	0.18μm	90nm	0.13μm	**90nm**
Architecture	Linear	Linear	Linear	**EER**

Performance comparison (LTE CMOS PAs)

	EuMW'12 B. Park et al.	ISSCC'13 K. Onizuka et	IMS'12 D. Kang et al.	This work
Frequency [GHz]	1.85	1.8	1.8	**1.95**
Modulation	10M 16QAM	20M 64QAM	10M 16QAM	**10M/ 20M 16QAM**
Output power [dBm]	26	21.3	26	**26/ 25.6**
Gain [dB]	~10	~13	~10	**29/ 28.1**
PAE [%] (w/o driver)	31.5	18	34	**37.2/ 35.3**
PAE [%] (w/ driver)	-	-	-	**34.1/ 32.2**
E-UTRA ACLR1 [dBc]	-32	-	-32.5	**-33.2/ -33**
Output transformer	off-chip	on-chip	off-chip	**on-chip**
Number of chips	1 chip	1 chip	2 chips	**1 chip**
Technology	0.18µm	65nm	0.18µm	**90nm**
Architecture	Linear	Supply path switching	Envelope tracking (ET)	**EER**

Conclusion

- High-efficiency fully integrated EER CMOS PA for WCDMA and LTE
- Envelope / phase generator based on MIX and limiter achieves wide BW phase path for low distortion
- Timing aligner based on DLL with variable HPF compensates for timing mismatch to obtain low distortion
- PAE and ACLR are 39.2% and -41.1dBc for WCDMA, and 32.2% and -33dBc for 20MHz-BW LTE

A Transformer-Coupled True-RMS Power Detector in 40nm CMOS

Brecht François and Prof. Patrick Reynaert

KU Leuven, ESAT-MICAS, Belgium

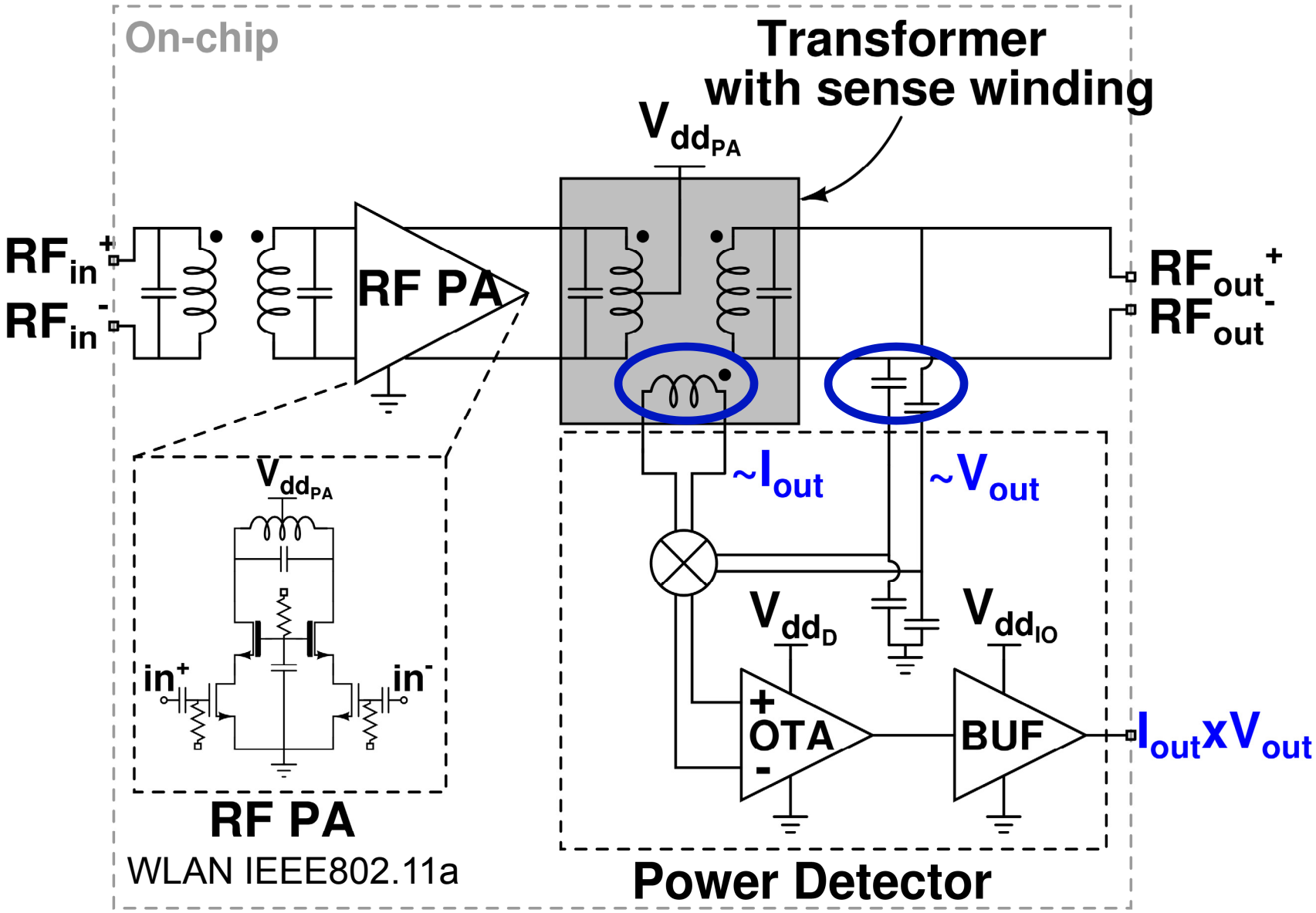
Outline

- Motivation
- Design
  - RF PA for WLAN IEEE802.11a at 5GHz
  - Transformer-coupled True-RMS power detector
- Measurement Results
- Conclusion

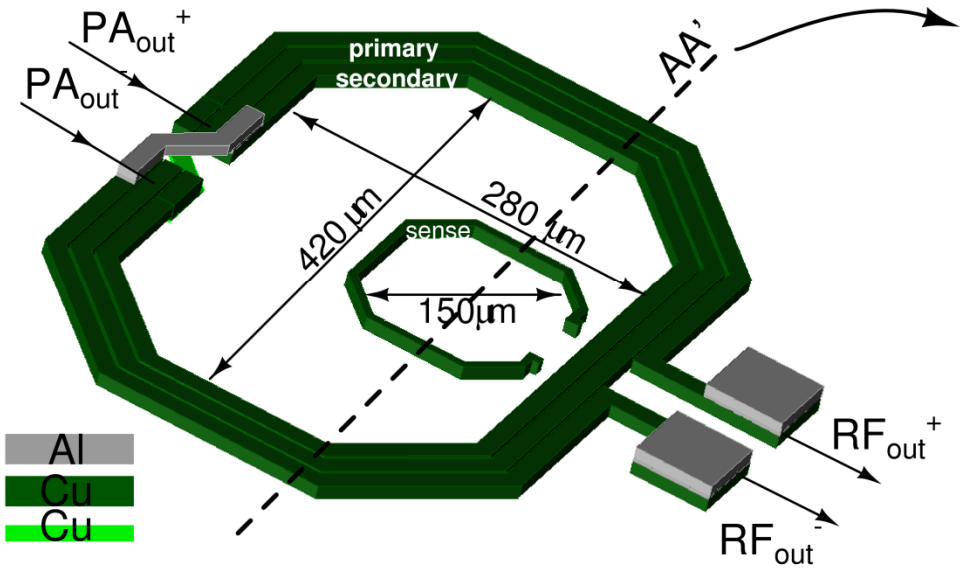
True-RMS Power Detection

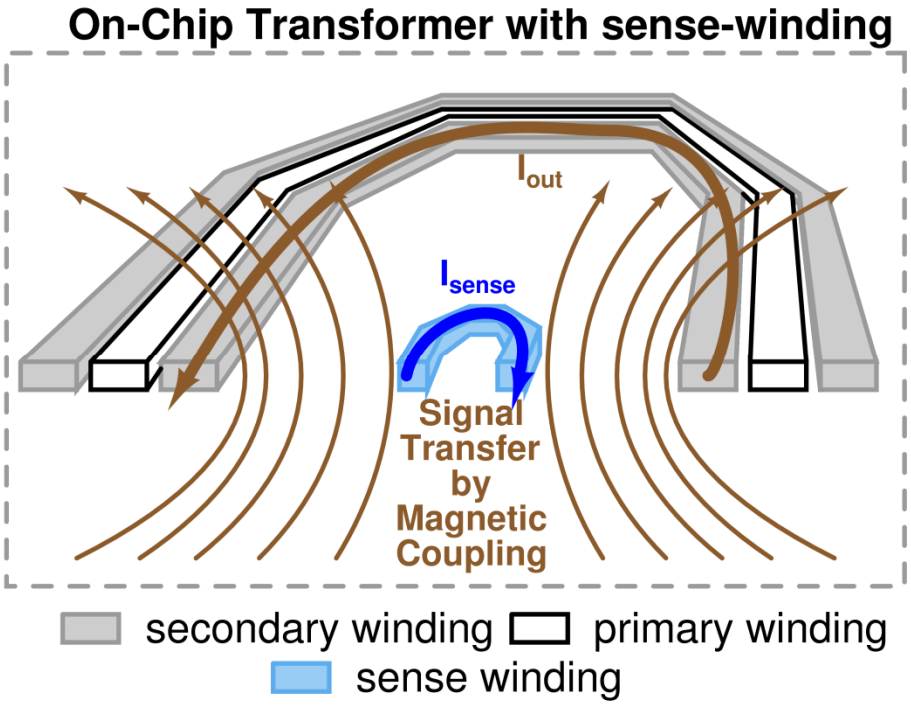
- Power → key requirement → communication
- Need:
  - On-chip RF power detector (PD)
    - compact design
    - low power consumption
  - True-RMS power detection
    - Load variations
    - VSWR

RF PA with Power Detector Architecture

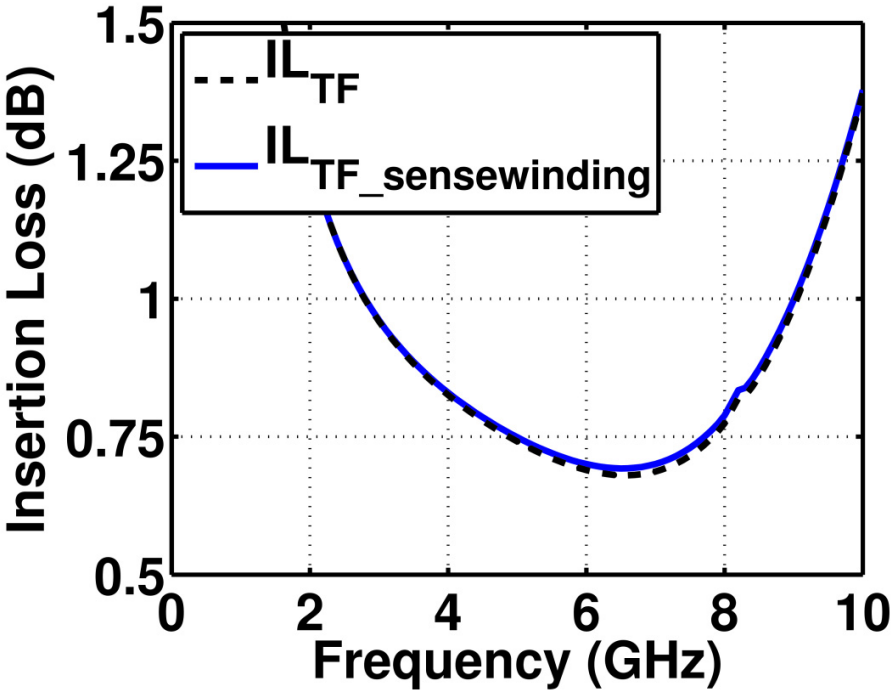


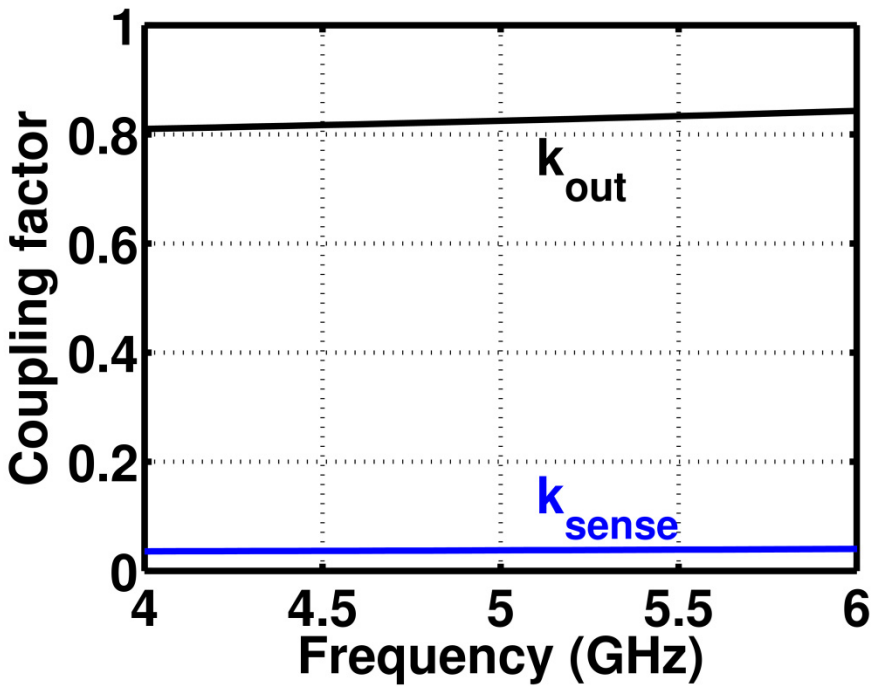
Designed Sense Winding



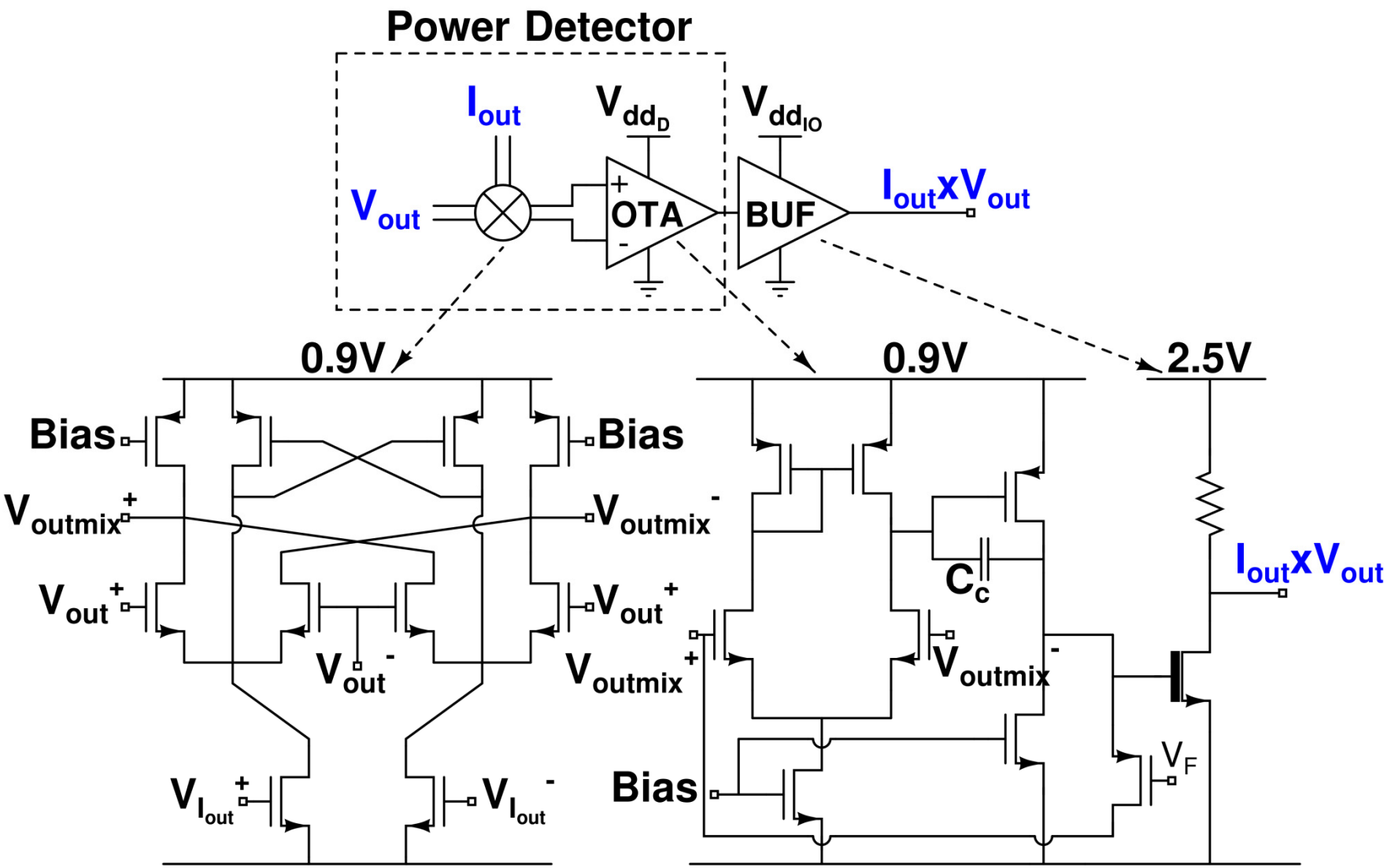


Designed Sense Winding

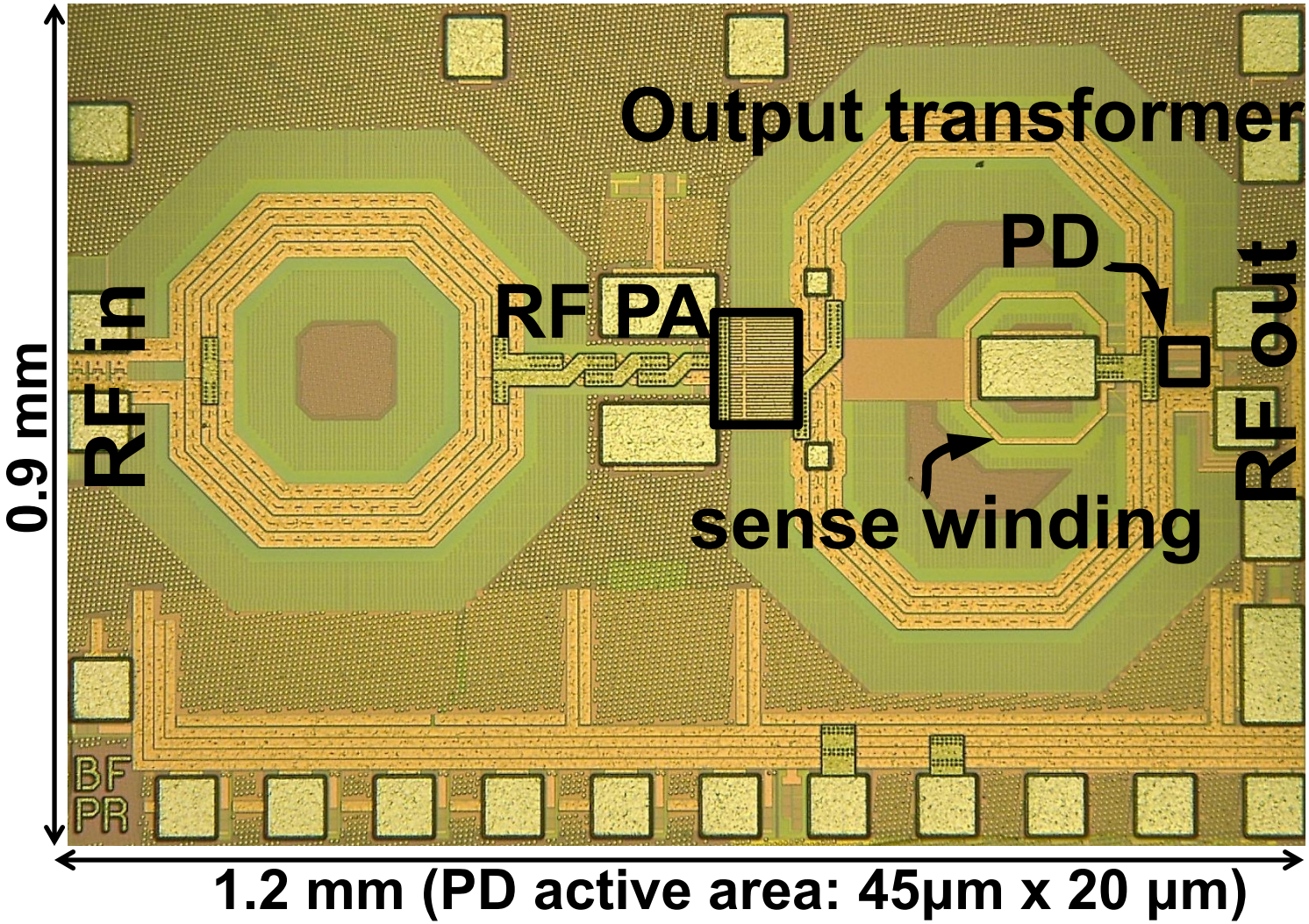




Power Detector Design



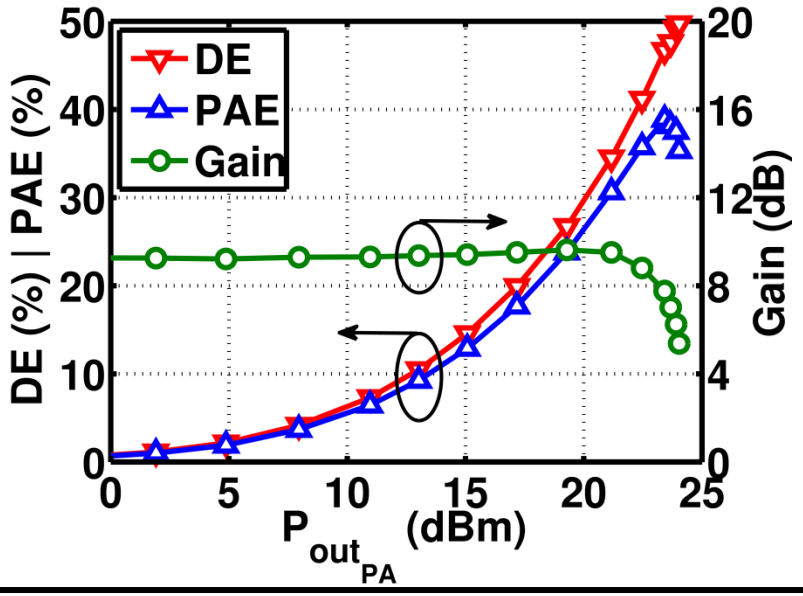
Die Micrograph

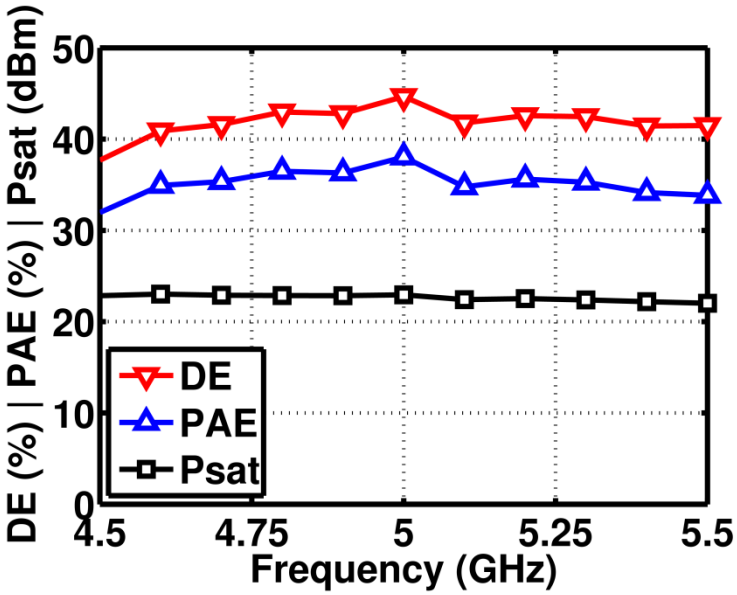


40 nm standard CMOS

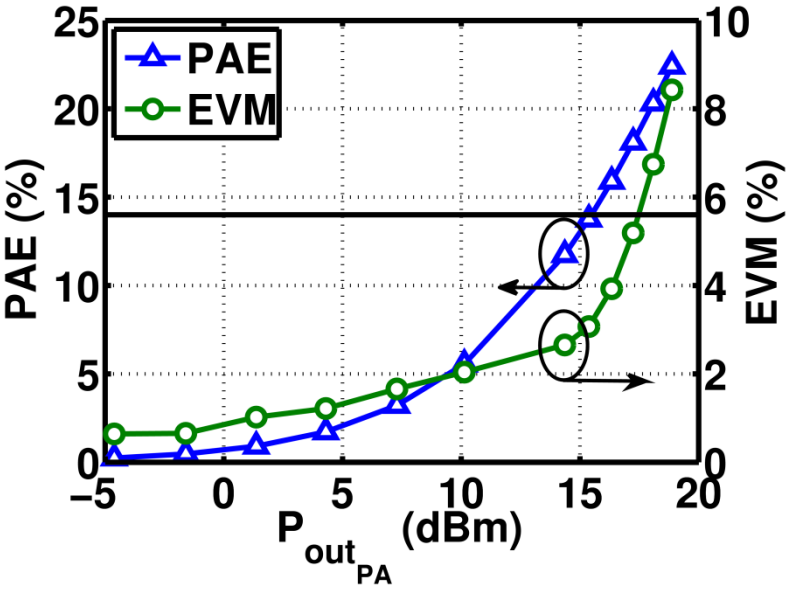
RF PA

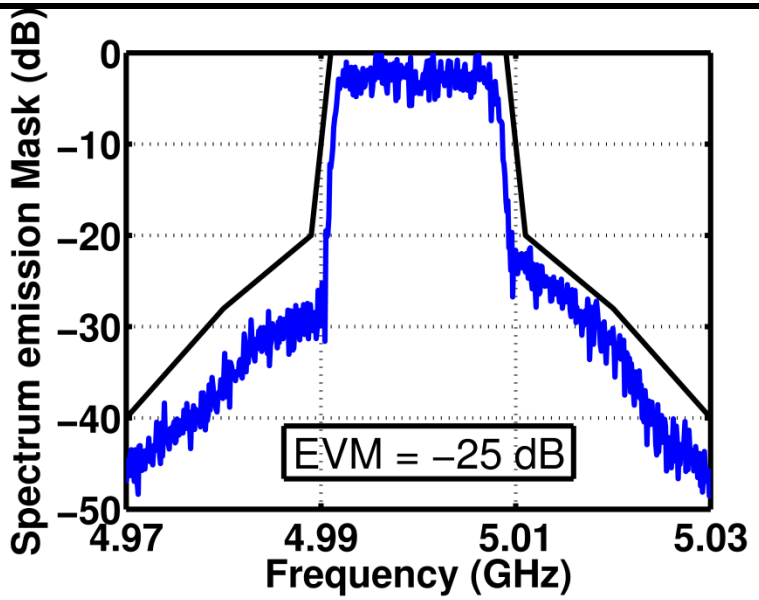
CW
5 GHz



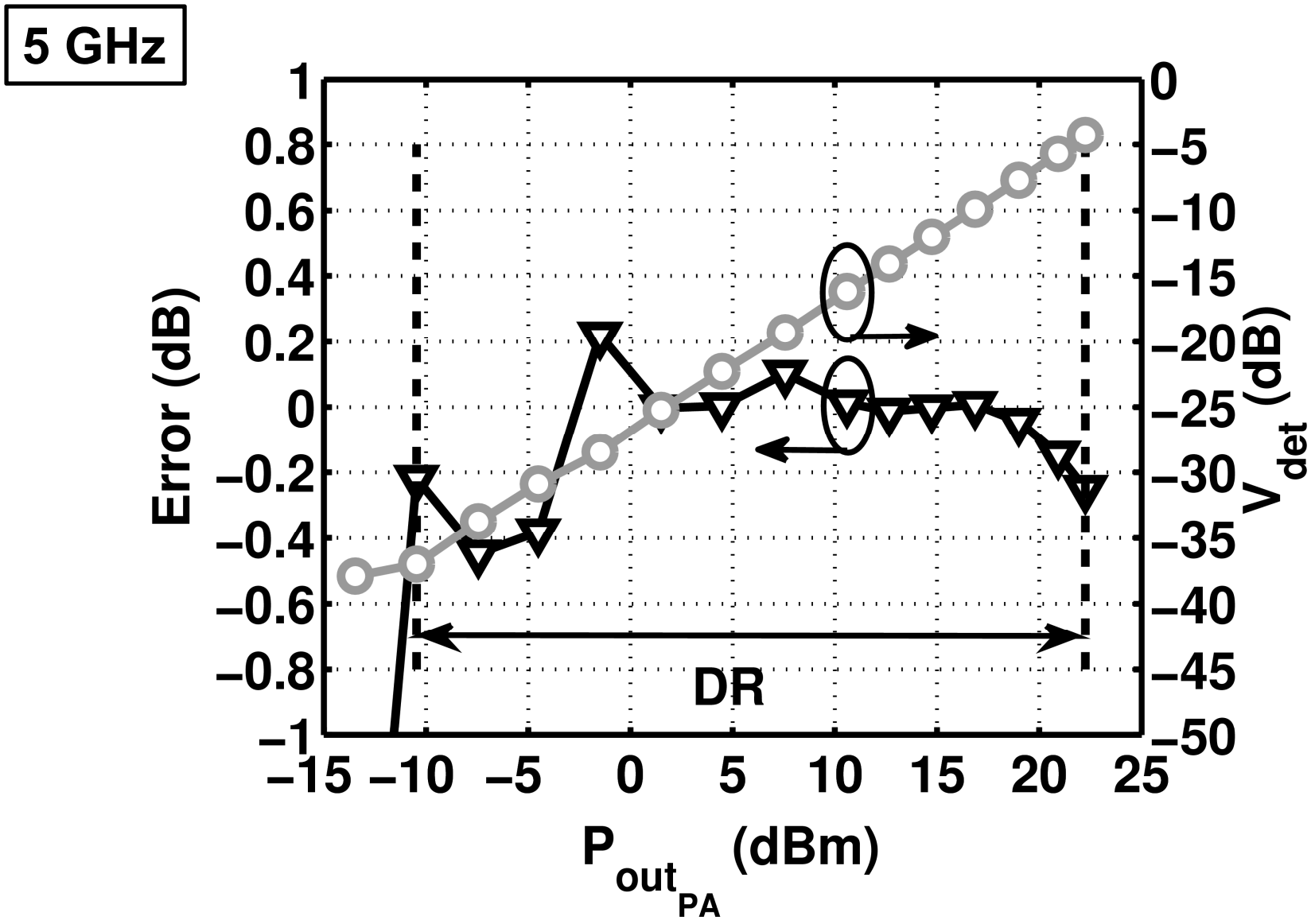


WLAN 802.11a
5 GHz 20 MHz
PAPR = 9.8 dB



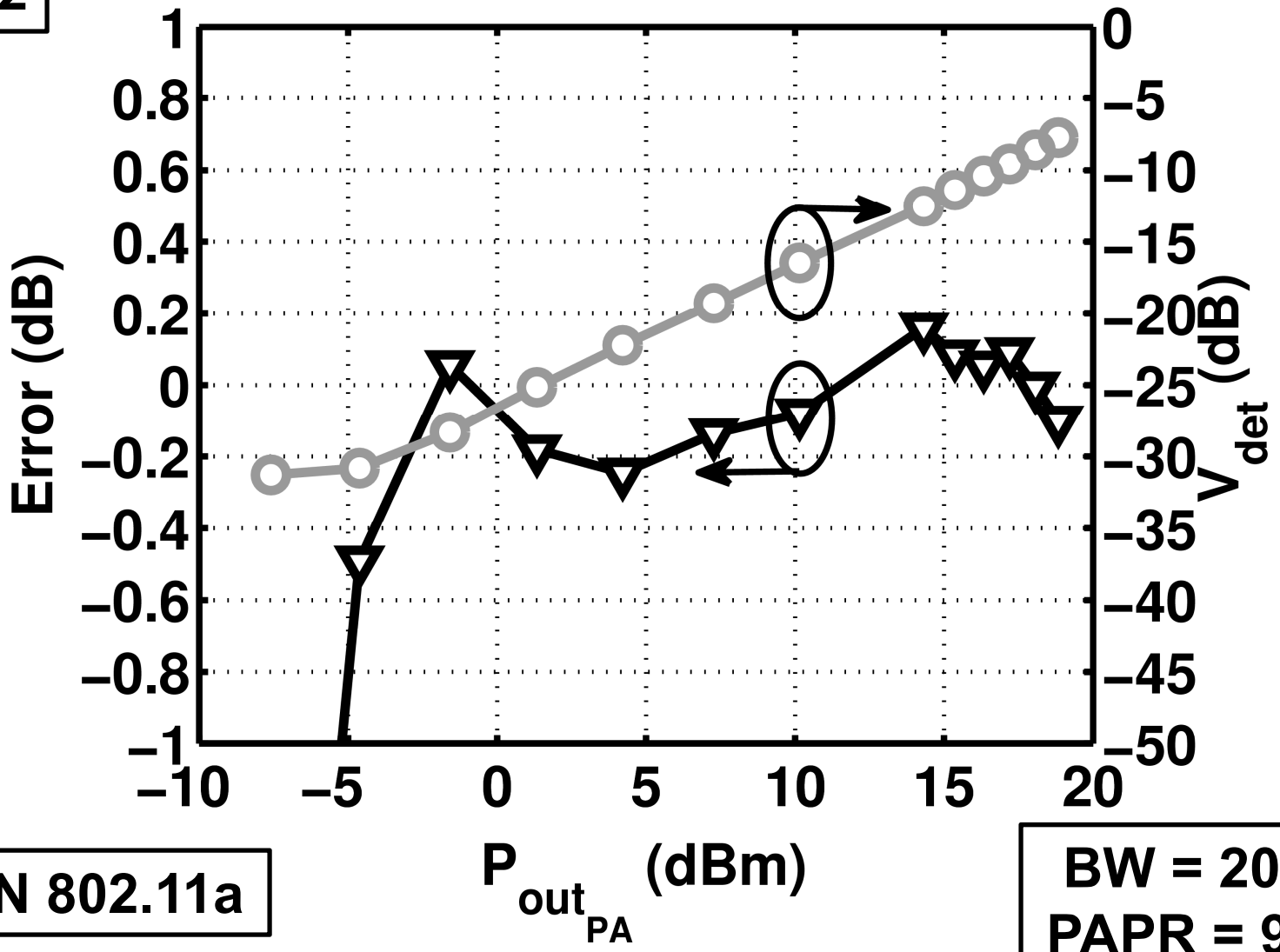


Power Detector Linearity - CW



Power Detector Linearity - WLAN

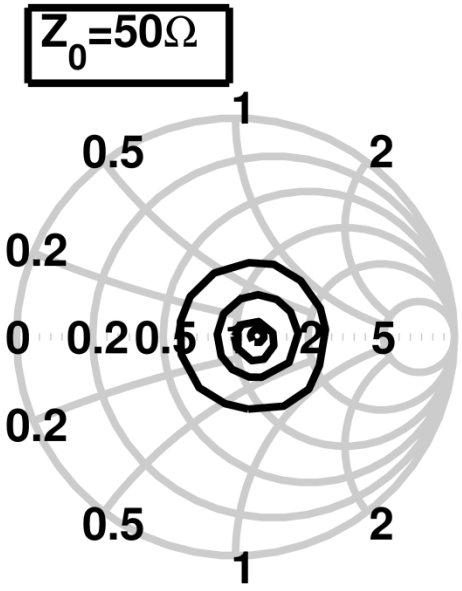
5 GHz



WLAN 802.11a

BW = 20 MHz
PAPR = 9.8 dB

Load Pull Measurements



VSWR 2.5:1
VSWR 1.8:1
VSWR 1.5:1
VSWR 1.3:1

Network Analyzer

ZVM

GPIB

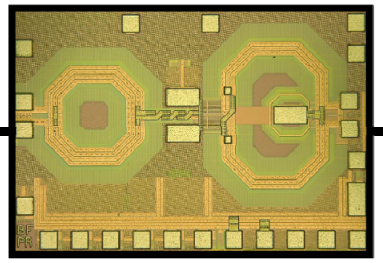
Power Meter

NRVS

Vector Signal Generator

SMBV 100A

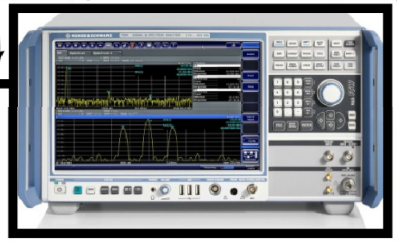
RF PA & PD



Impedance Tuner

Maury 8045p

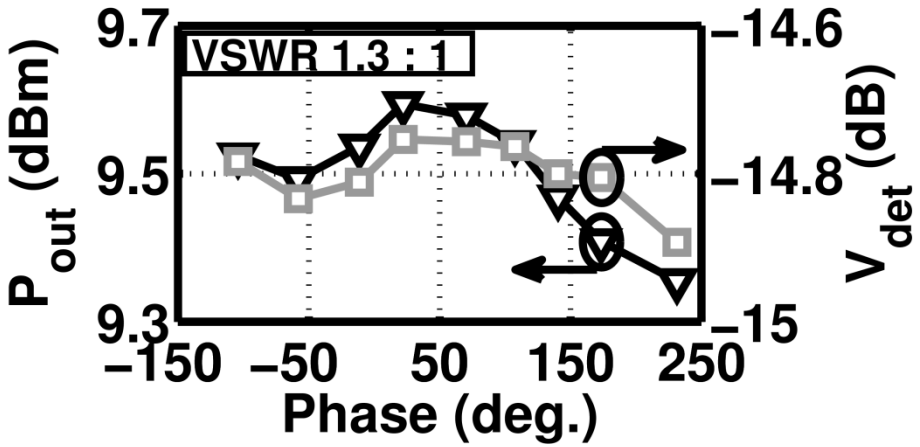
Signal Analyzer

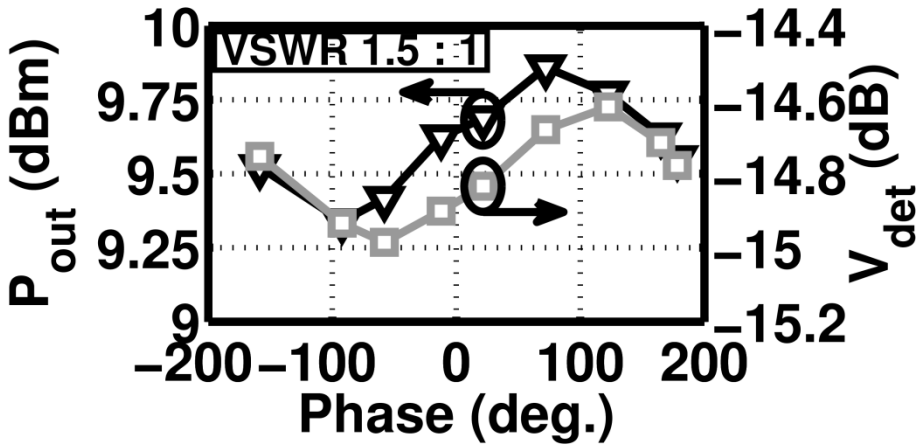


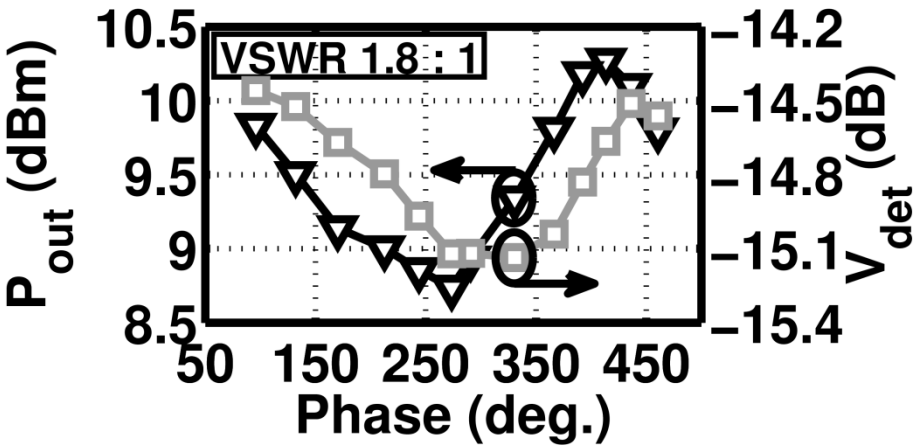
FSW 43

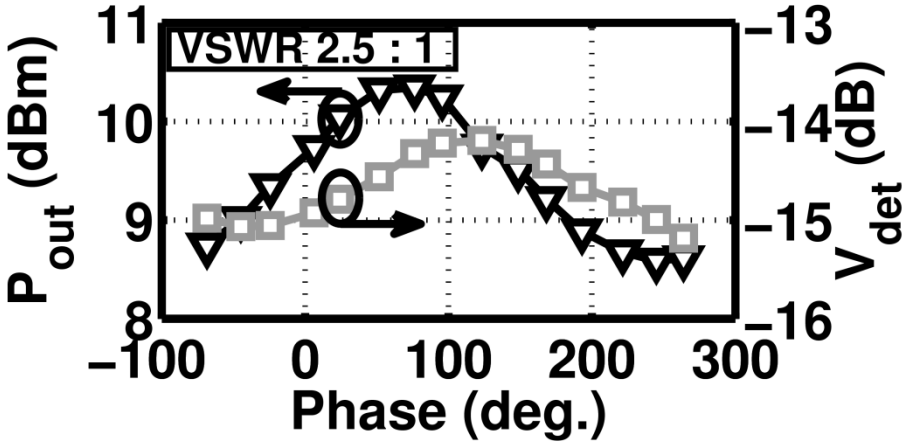
Load Pull Measurements

5 GHz

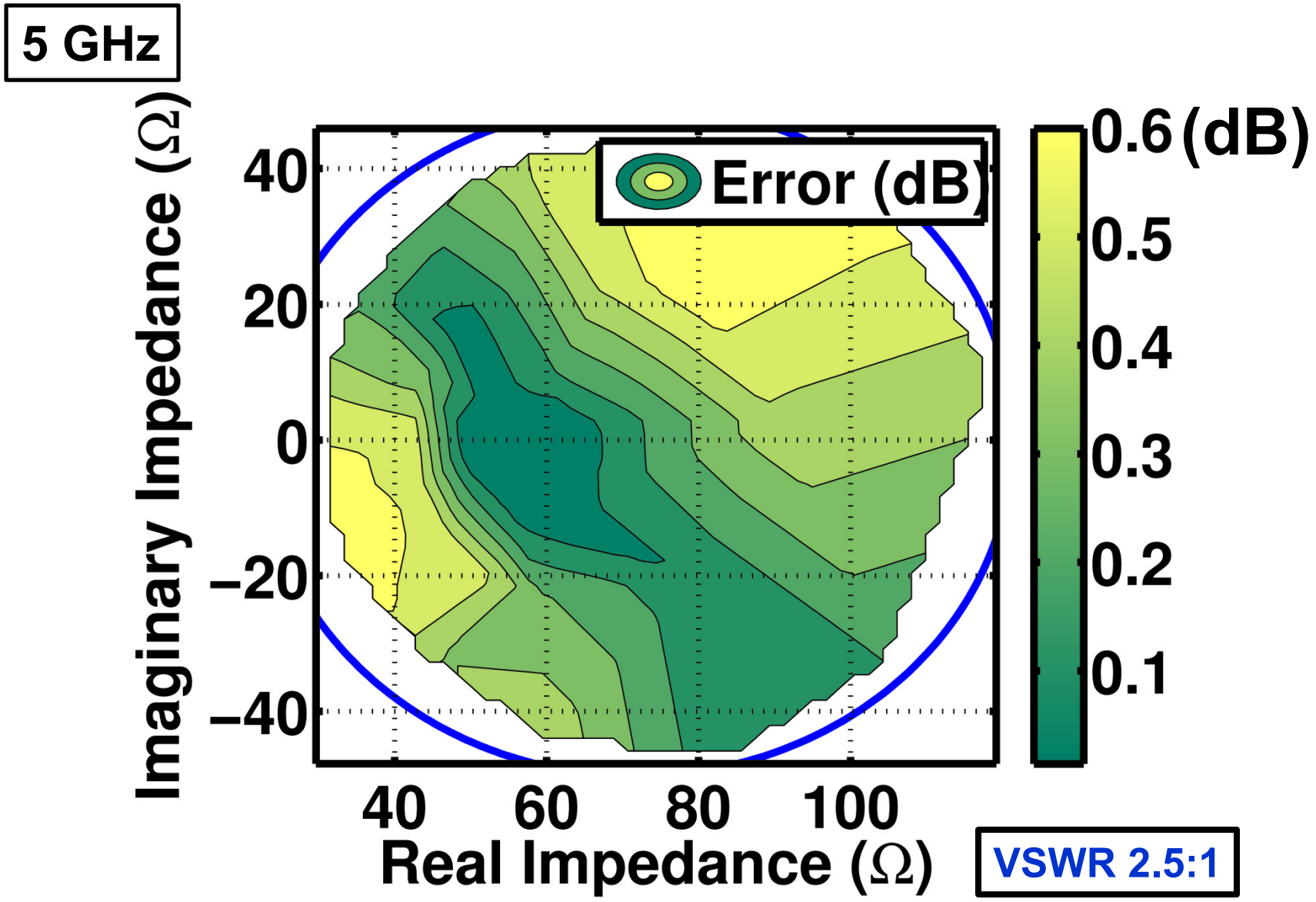




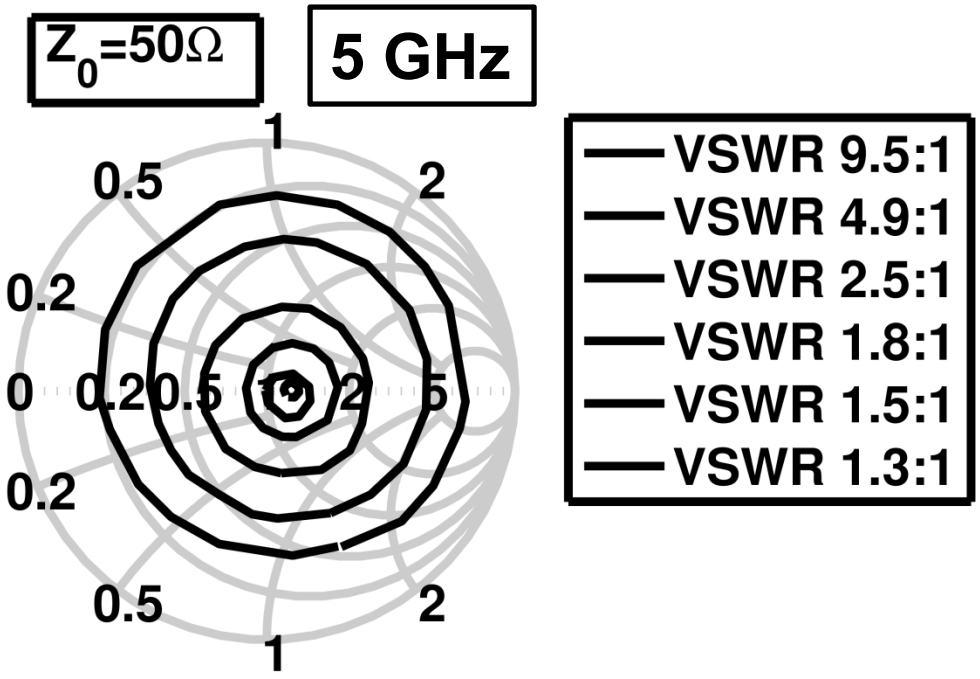




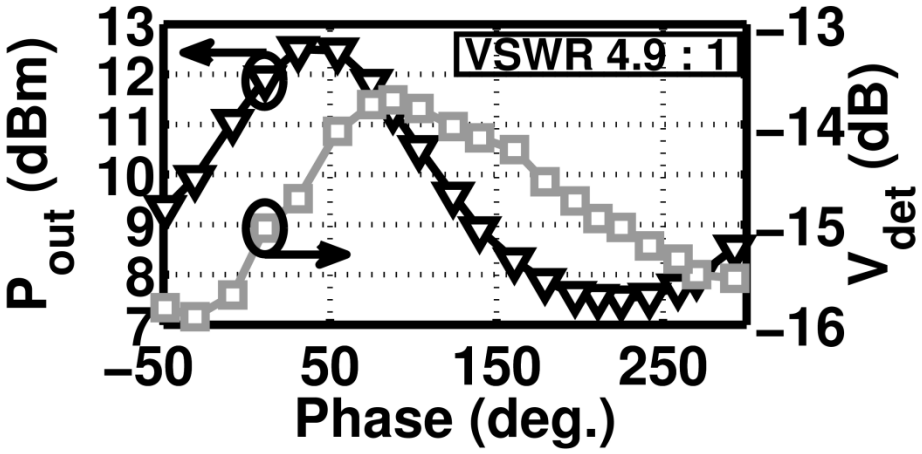
Load Pull Measurements

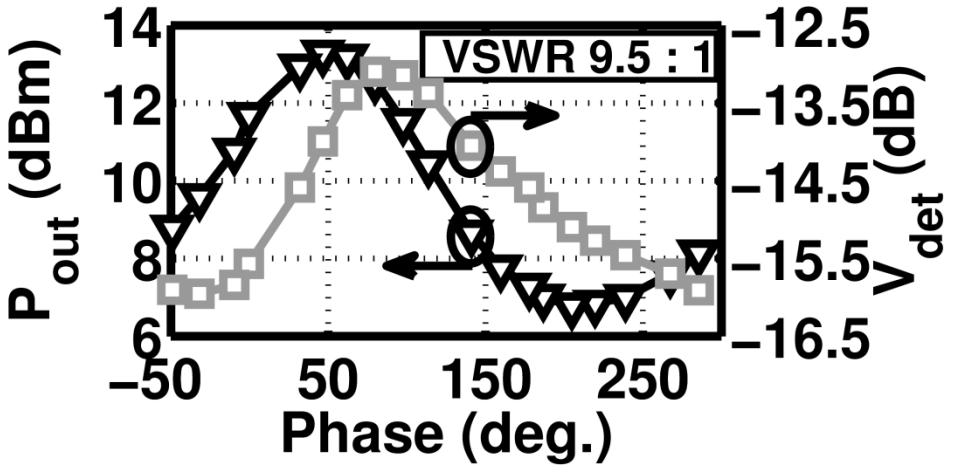


Load Pull Measurements



- Sense winding is affected by current in primary winding
- Thus: results in Error
- Solution: making extra calculations





Comparison

	[1] MTT'08 Zhou	[2] JSSC'09 Townsend	[3] ESSCIRC'10 Gorisse	[4] TIM'09 Chaojiang	[5] ESSCIRC'12 Nakamoto	**This work**
CMOS Technology	130 nm	180 nm	65 nm	130 nm	90 nm	**40 nm GP**
PA integrated	No	No	No	No	Yes	**Yes**
Coupling topology	Capacitive	Capacitive	Capacitive	Capacitive	Capacitive	**Capacitive & Inductive**
Detector Principle	Voltage	Voltage	Voltage	Voltage	Voltage	**Voltage & Current**
Power consumption [mW]	0.18	3.8	0.06	0.12	0.3-0.63	**0.31**
Dynamic Range [dB]	20	20	25	21	27	**32.5**
Linearity Error [dB]	±0.5	±2.4	-	±1%	±0.5	**±0.5**
Error under VSWR mismatch [dB]	-	-	-	-	-	**±0.6**
Active Area [μm^2]	12600	360000	6400	85000	39000	**900**
Area Overhead	Yes	Yes	Yes	Yes	Yes	**No**

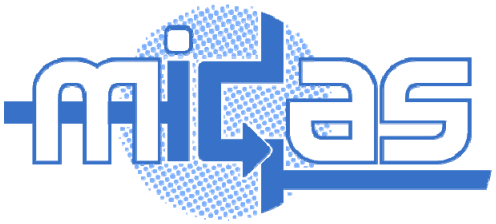
Conclusion

- Fully integrated RF PD in 40nm CMOS (900 μm^2)
  - Current
  - Voltage
- Integrated together with RF PA for IEEE 802.11a at 5GHz
- Transformer-coupled true-RMS power detector for varying load impedances

A Dual-Mode Transformer-Based Doherty LTE Power Amplifier in 40 nm CMOS

Ercan Kaymaksüt and Prof. Patrick Reynaert

KU LEUVEN



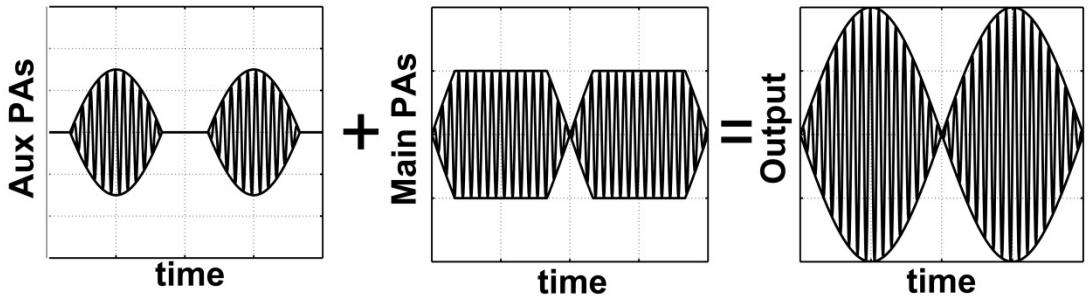
KU Leuven, ESAT-MICAS, Belgium

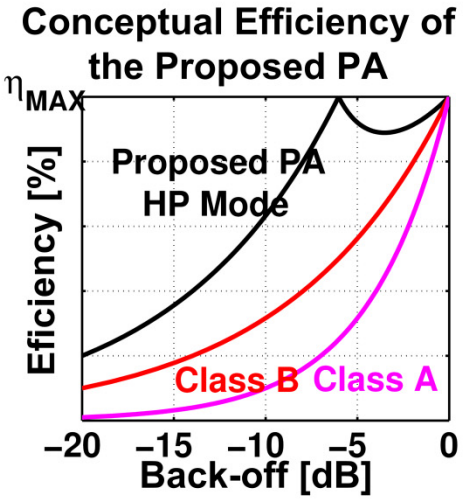
LTE PA Design in nano-scale CMOS

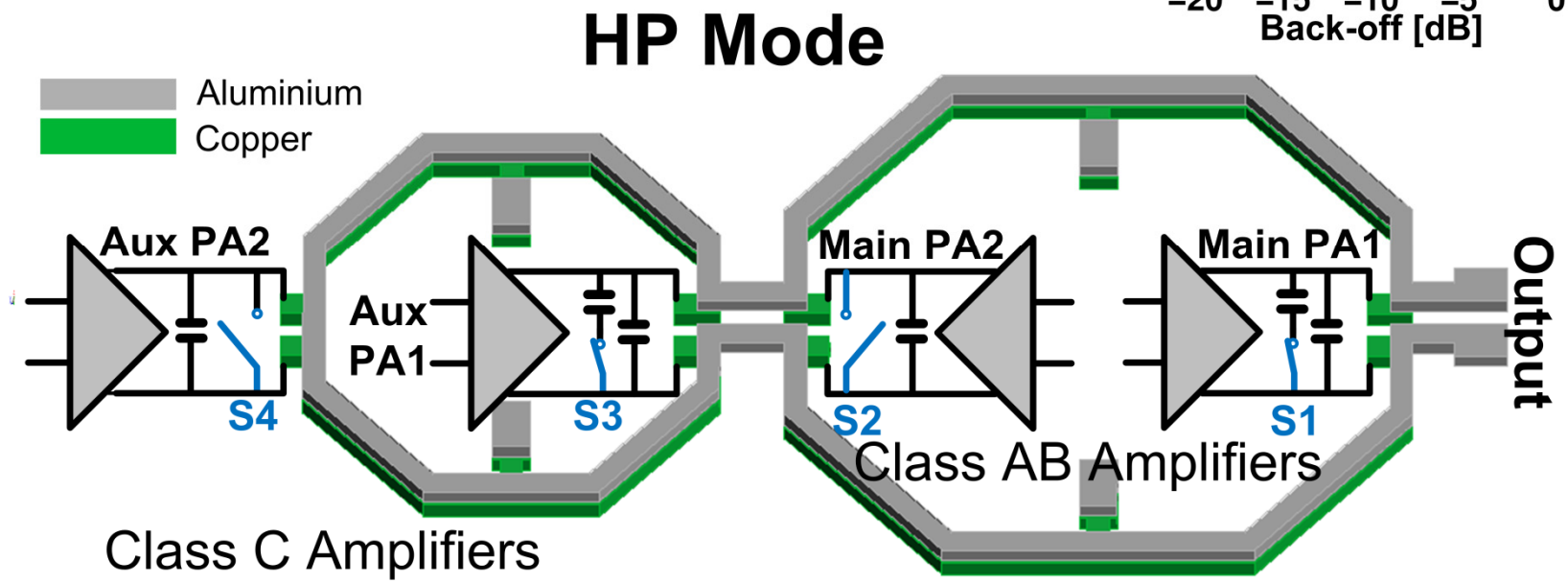
- Goals
  - High output power (P_{ave}>23 dBm)
  - LTE compliant linearity
  - High back-off efficiency

- Challenges
  - Low breakdown voltage transistors
  - Low Q inductors on silicon substrate

Architecture: Dual-Mode Doherty (1)

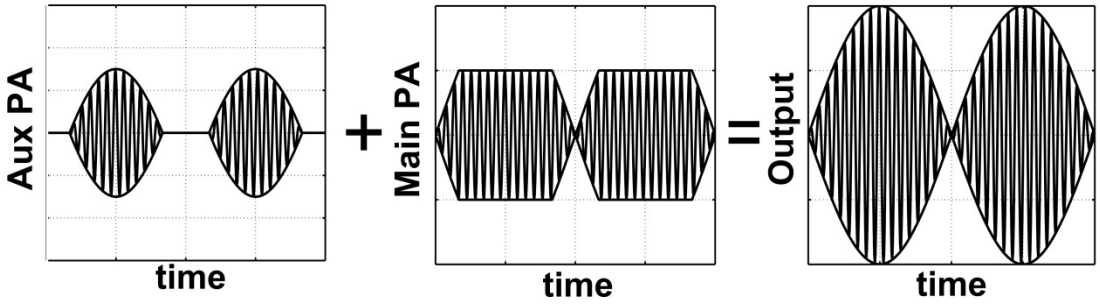


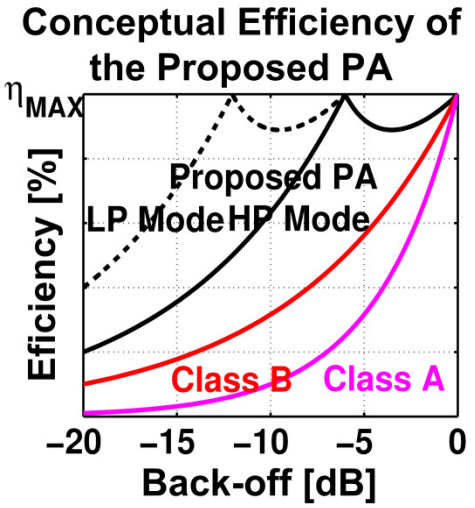


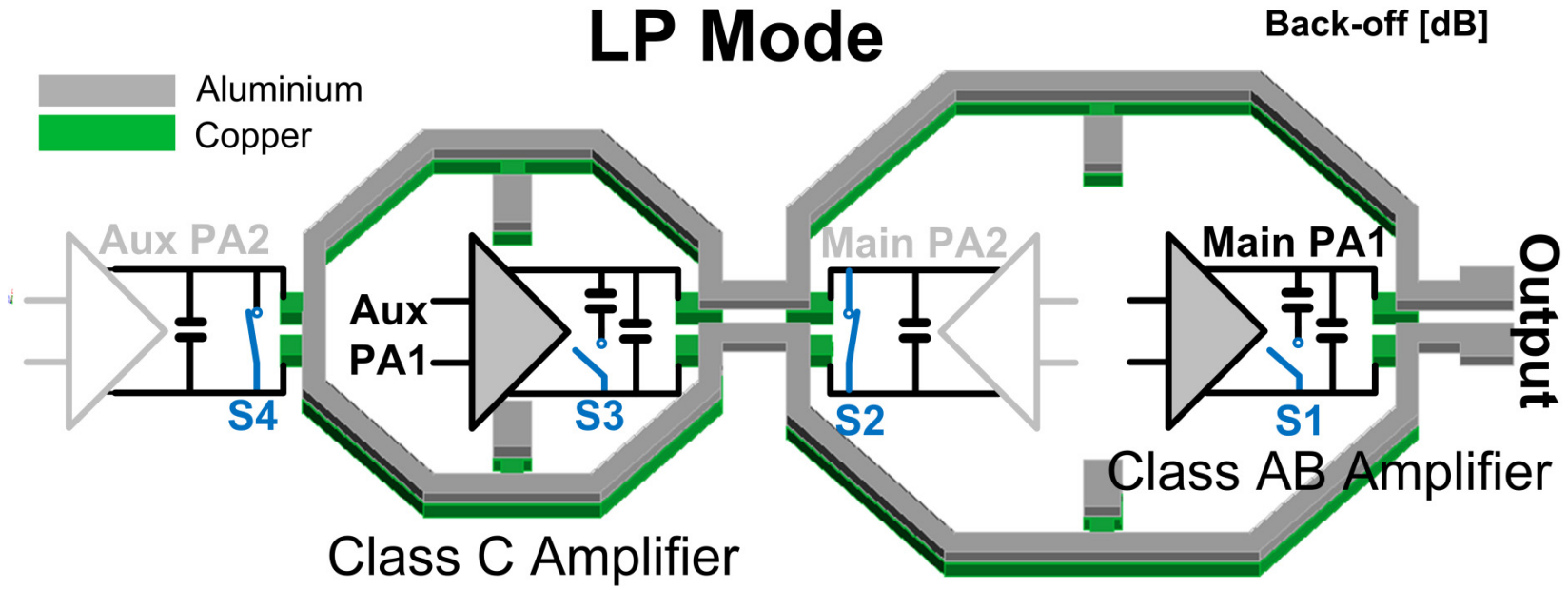


- Main PAs saturate at 6 dB back-off with high efficiency

Architecture: Dual-Mode Doherty (2)

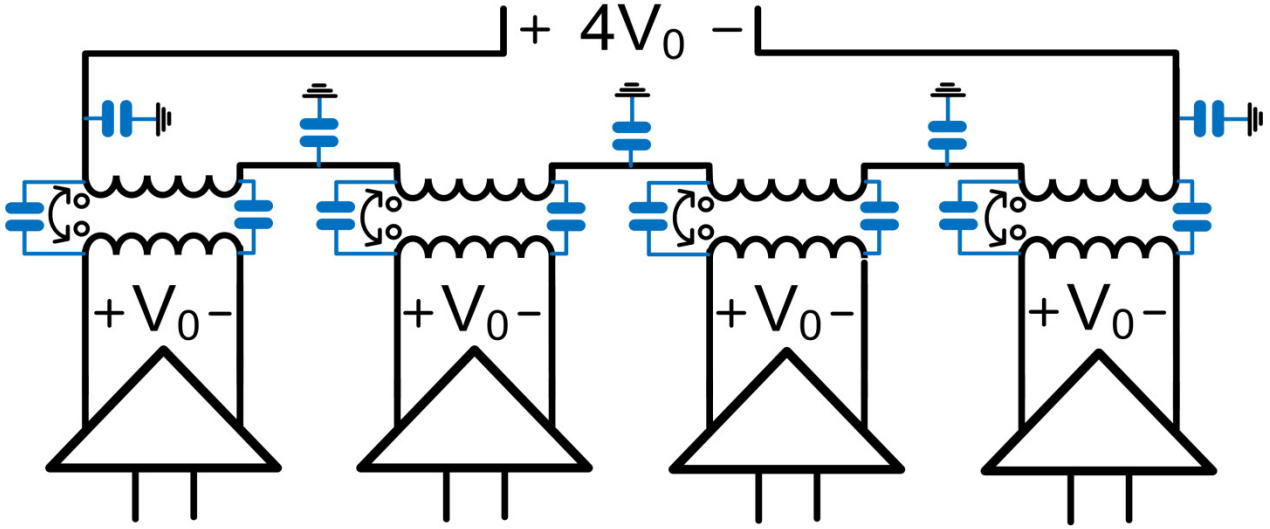






- Only 1 Main PA and 1 Aux PA operate at Low Power Mode

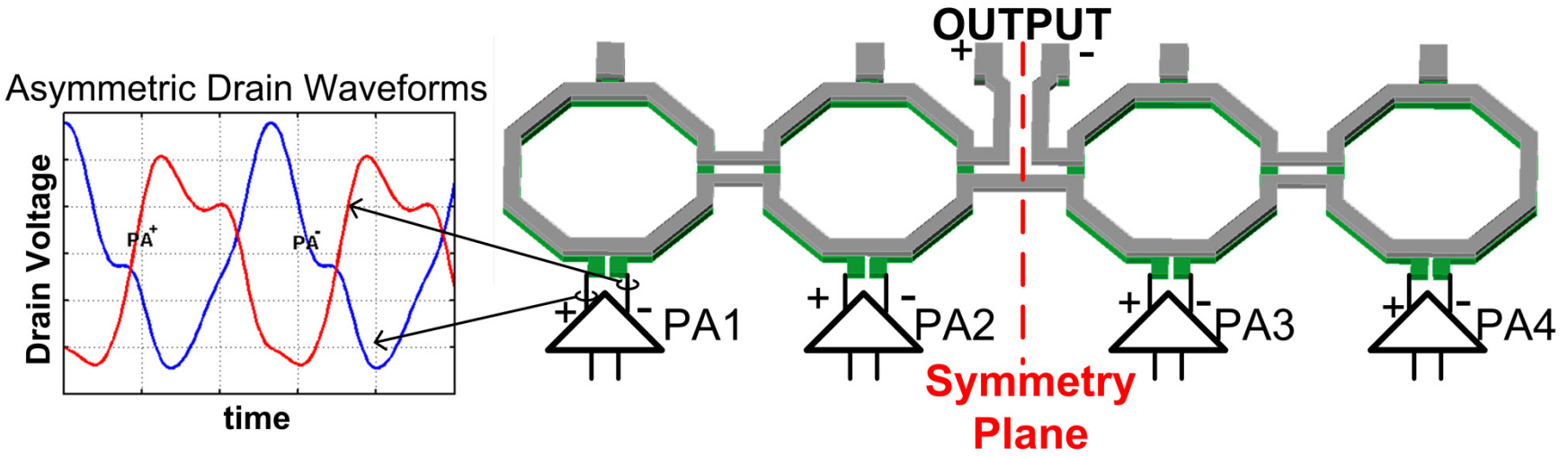
Series Combining Transformers



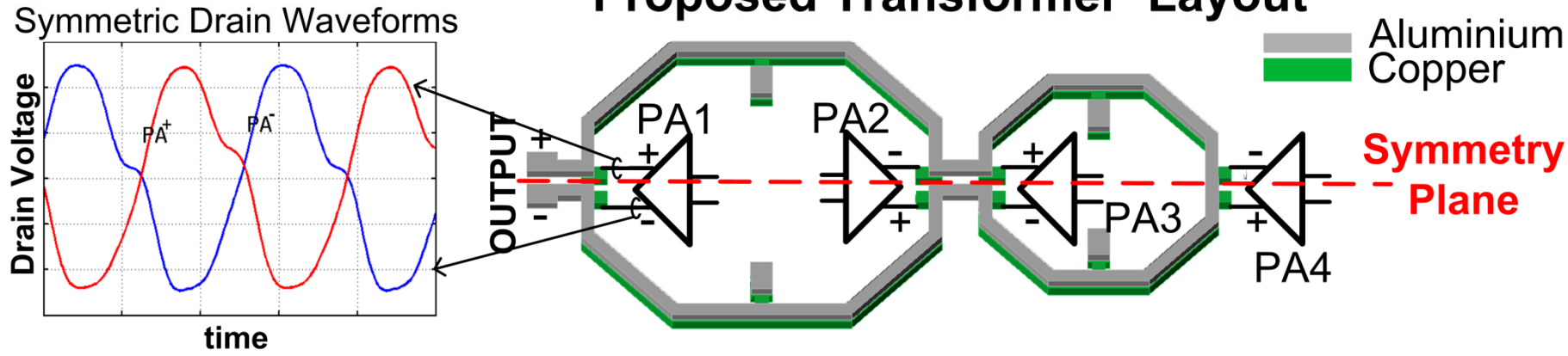
- Advantages
  - Wide bandwidth
  - Low loss
  - Reconfigurable
- Potential Disadvantage
  - The parasitic capacitors ***might*** cause asymmetry in the push-pull amplifiers

Asymmetry in Transformer Combiners

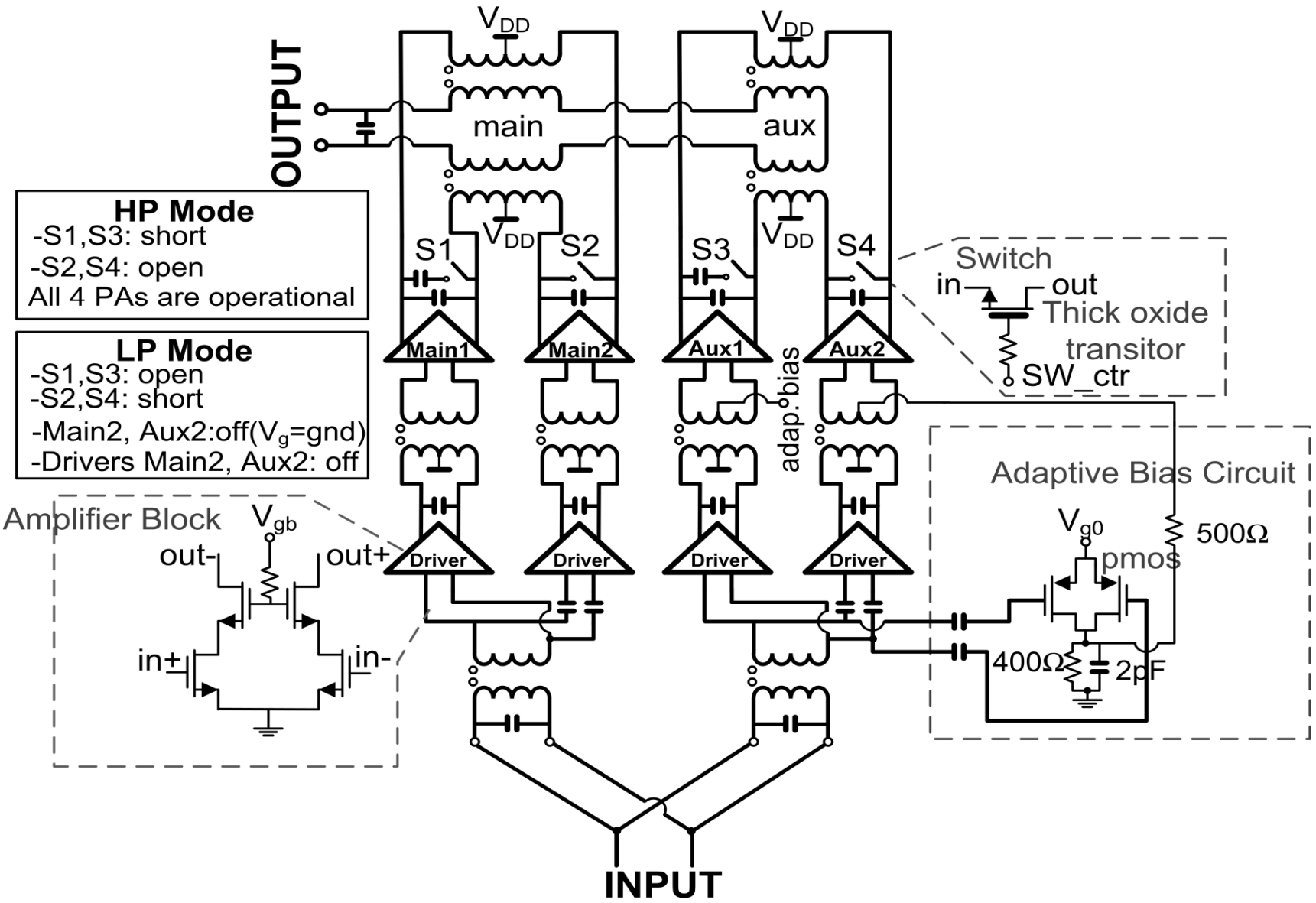
Conventional Figure-8 shaped Transformer Layout



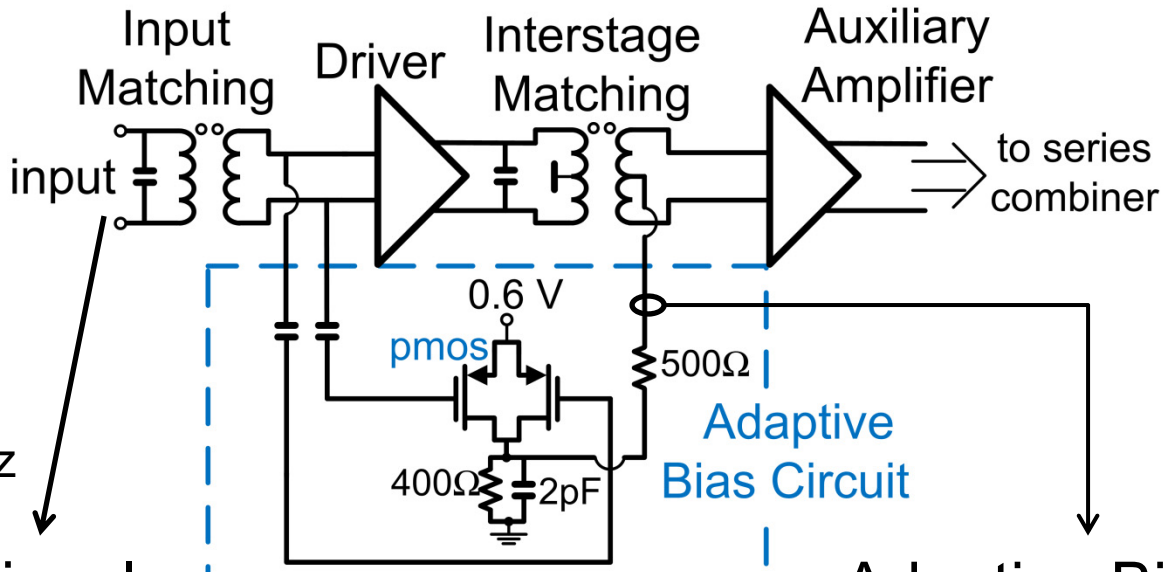
Proposed Transformer Layout



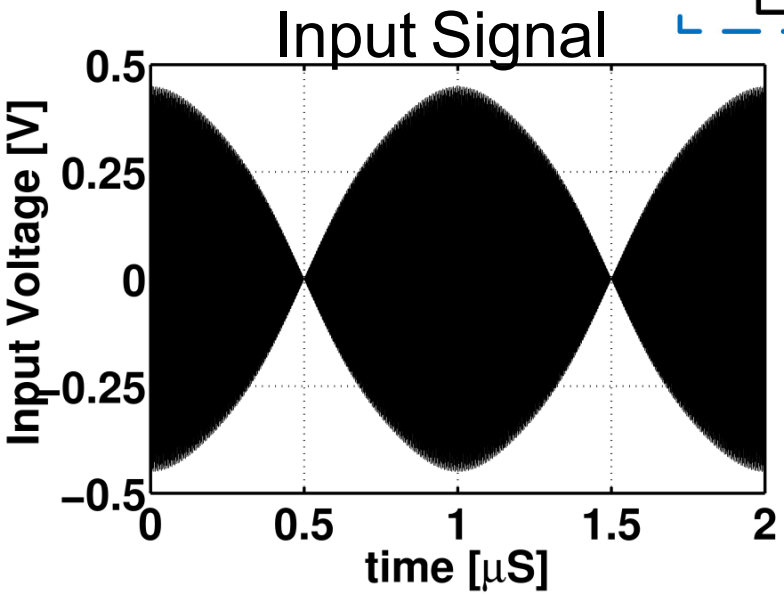
Schematic

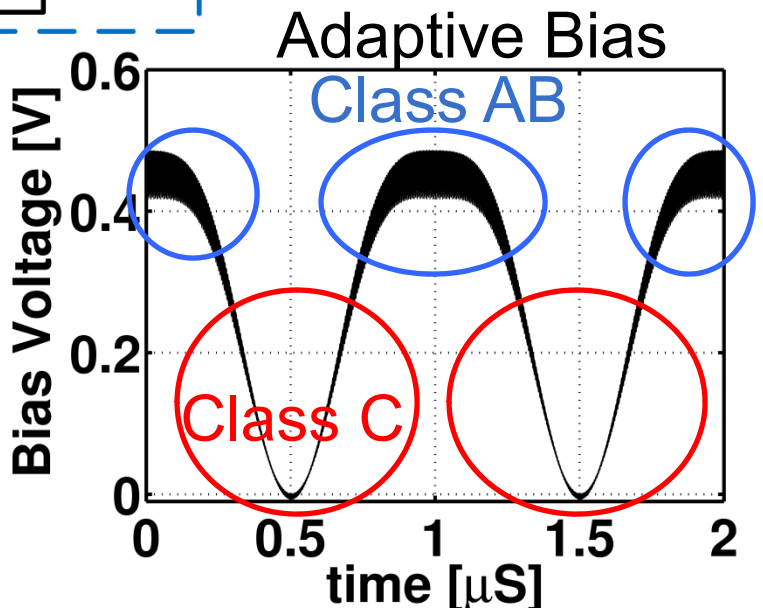


Adaptive Bias Circuit

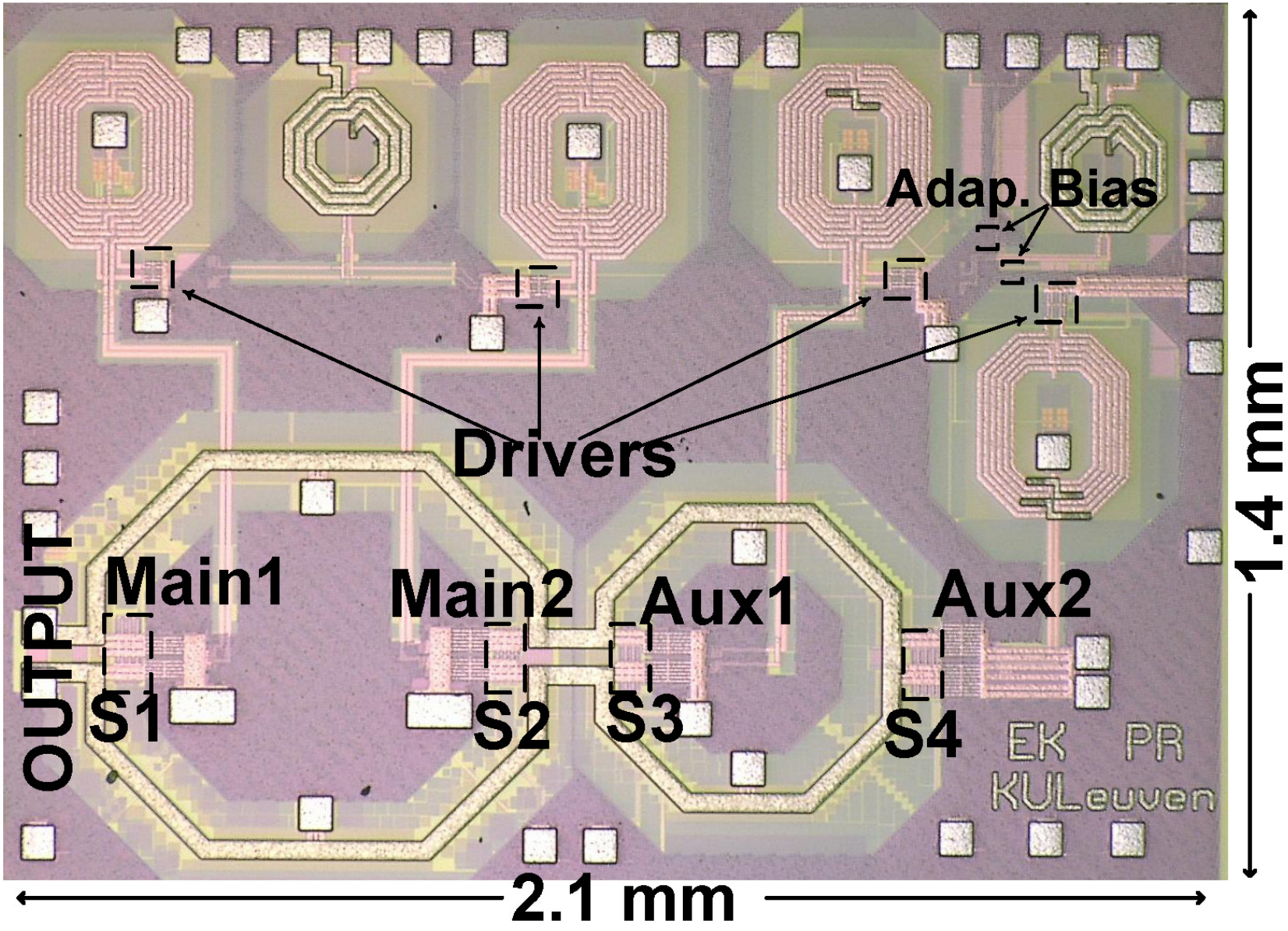


two tone signal
f_0: 1.9 GHz
tone spacing: 1 MHz



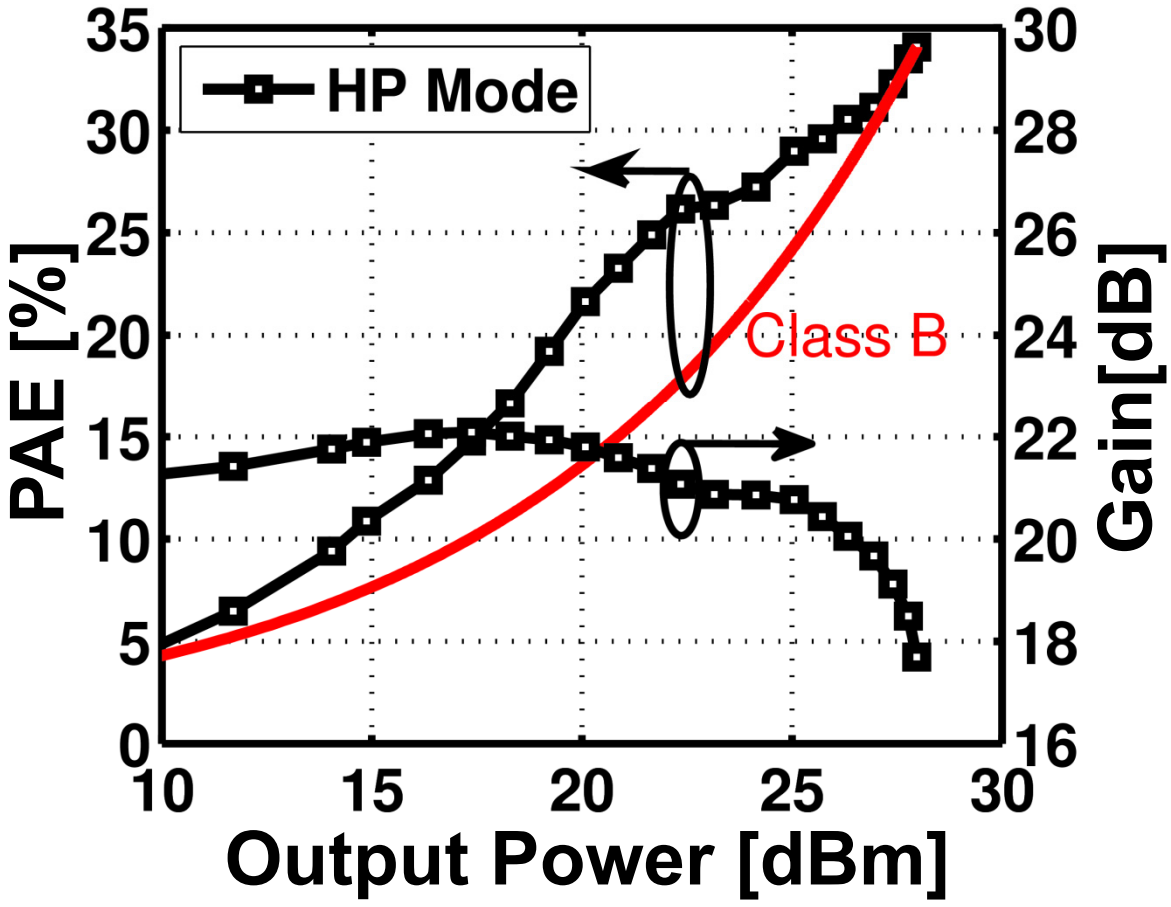


Die Photo



Measurement Results-CW (1)

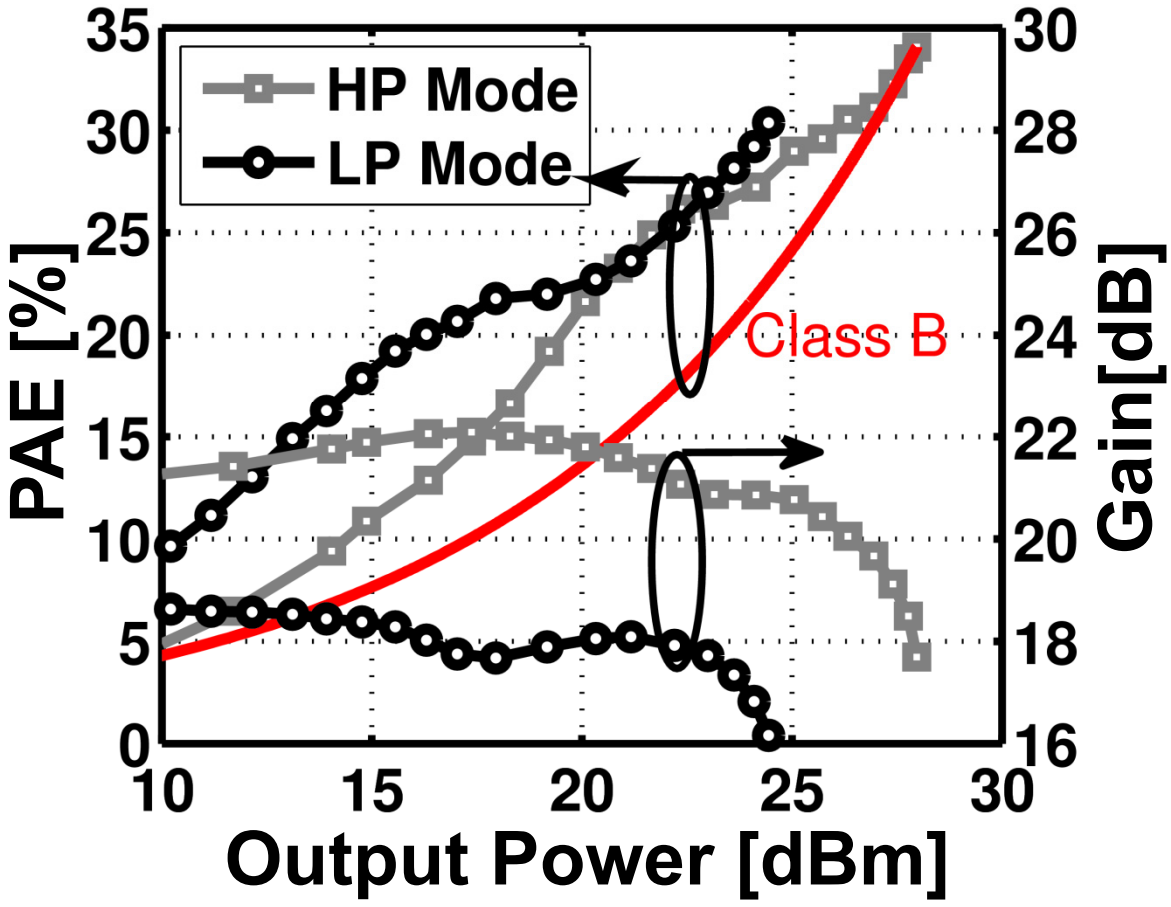
CW Measurements at 1.9 GHz



- P_{SAT}: 28 dBm
- PAE@P_{SAT}: 34%
- PAE@6dB back-off: 25.5% (HP Mode)

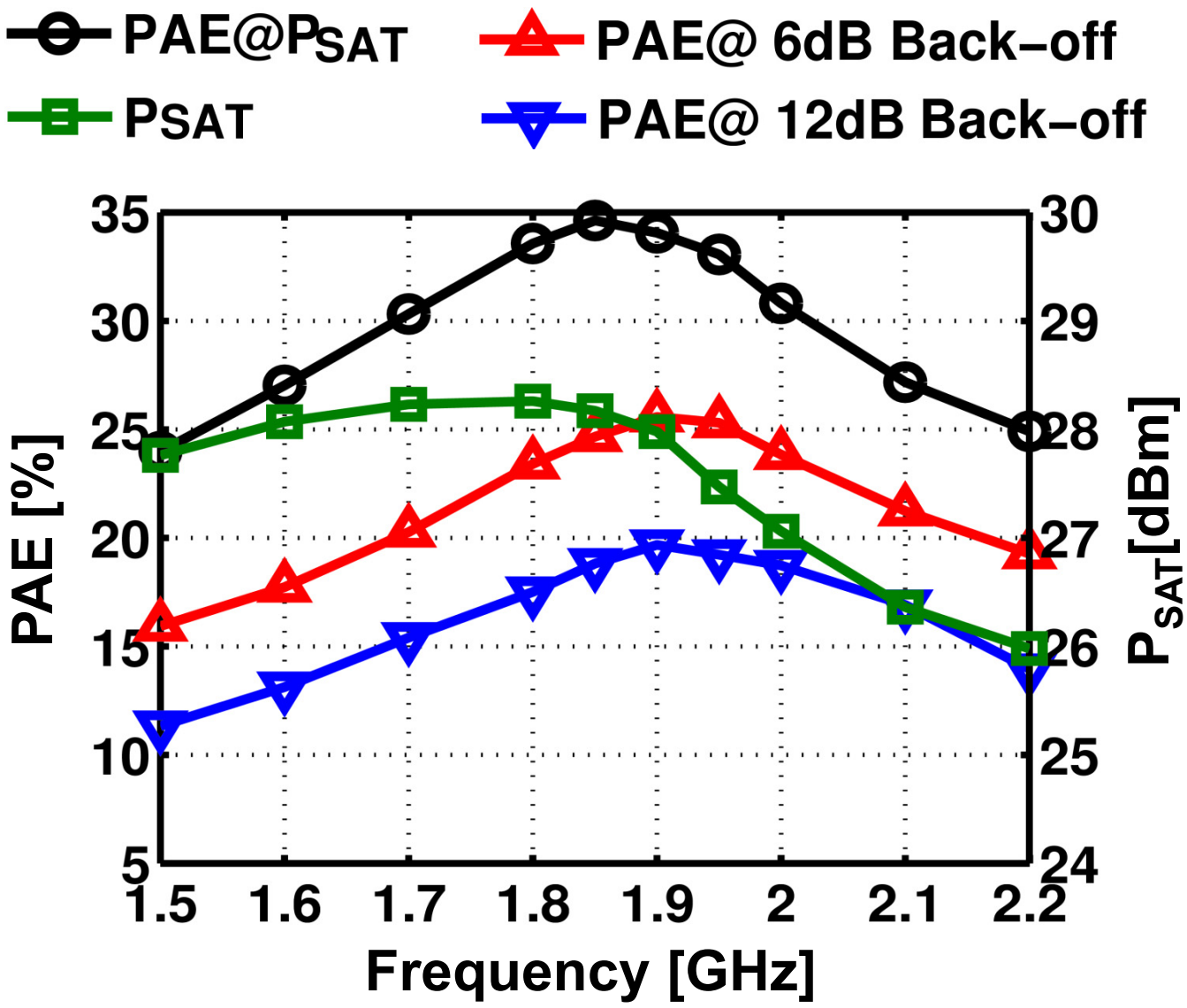
Measurement Results-CW (2)

CW Measurements at 1.9 GHz

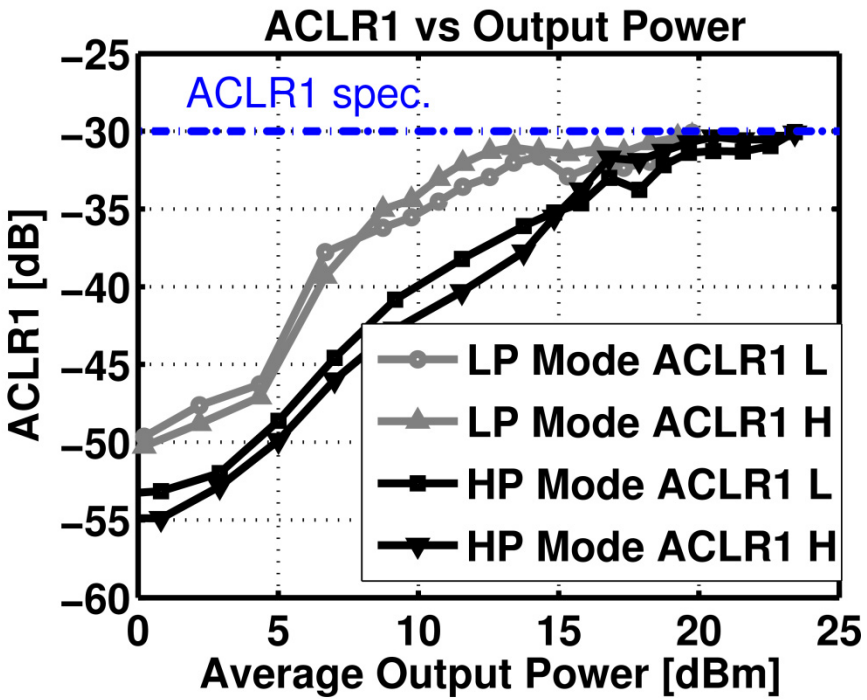


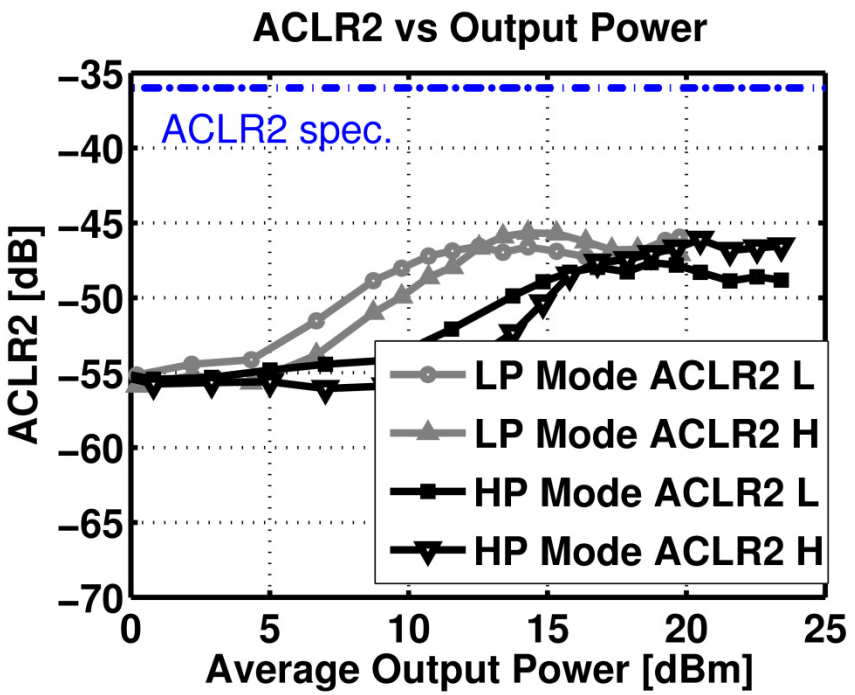
- P_{SAT}: 28 dBm
- PAE@P_{SAT}: 34%
- PAE@6dB back-off: 25.5% (HP Mode)
- PAE@12dB back-off 19.7% (LP Mode)

Measurement Results-Frequency Response

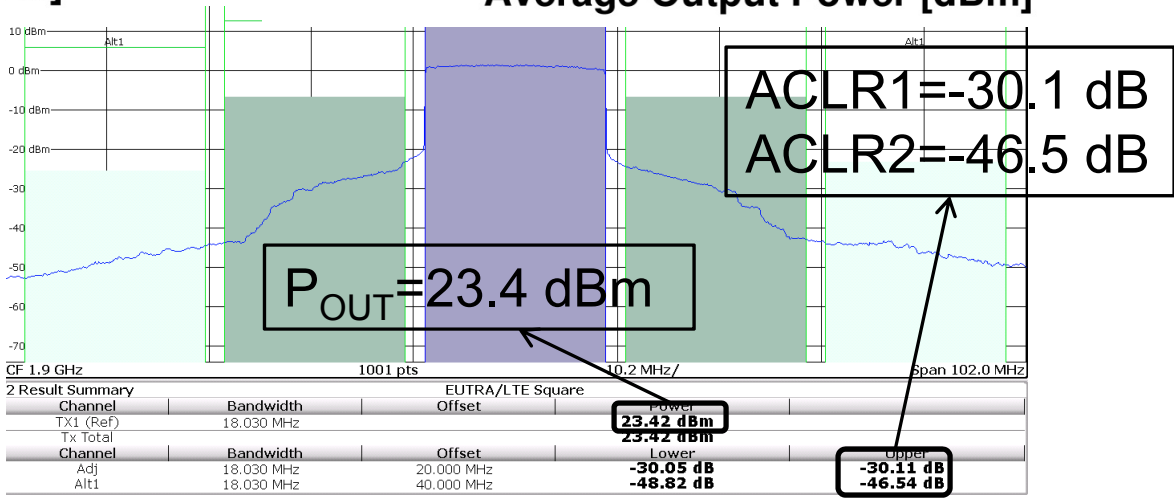


Measurement Results- LTE (1)



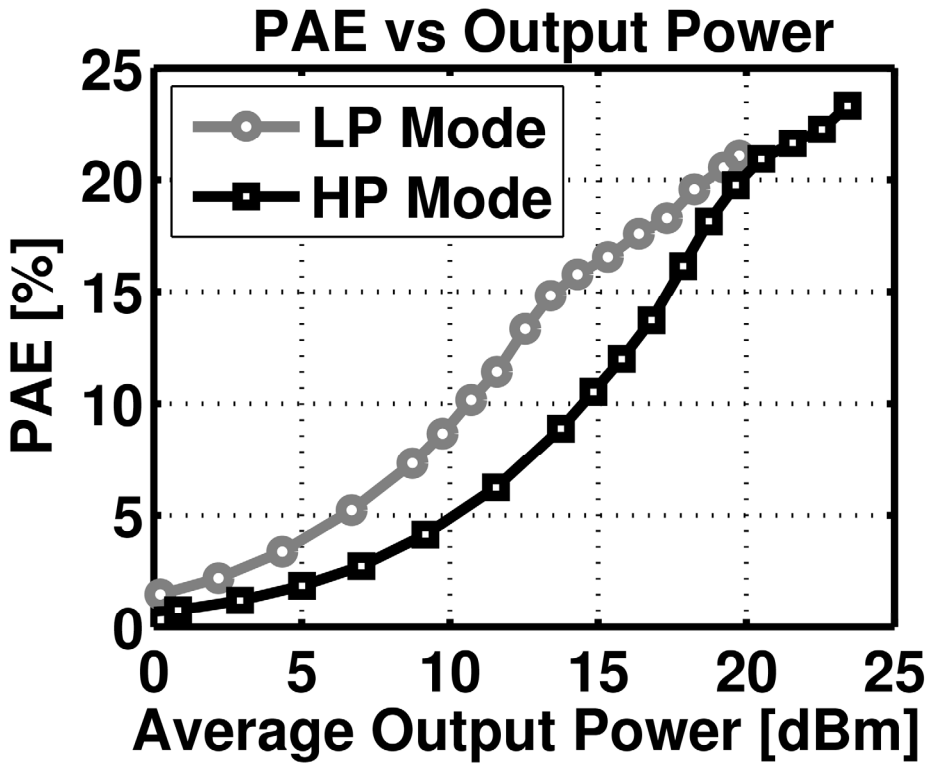


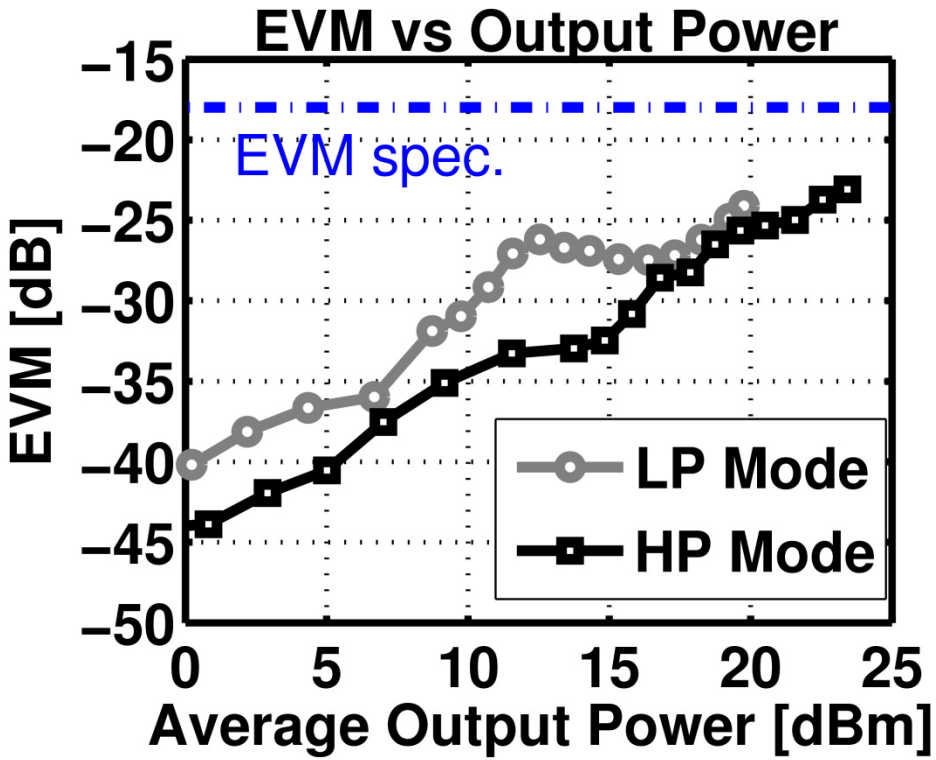
- 20 MHz 16 QAM LTE signal at 1.9 GHz
- without predistortion



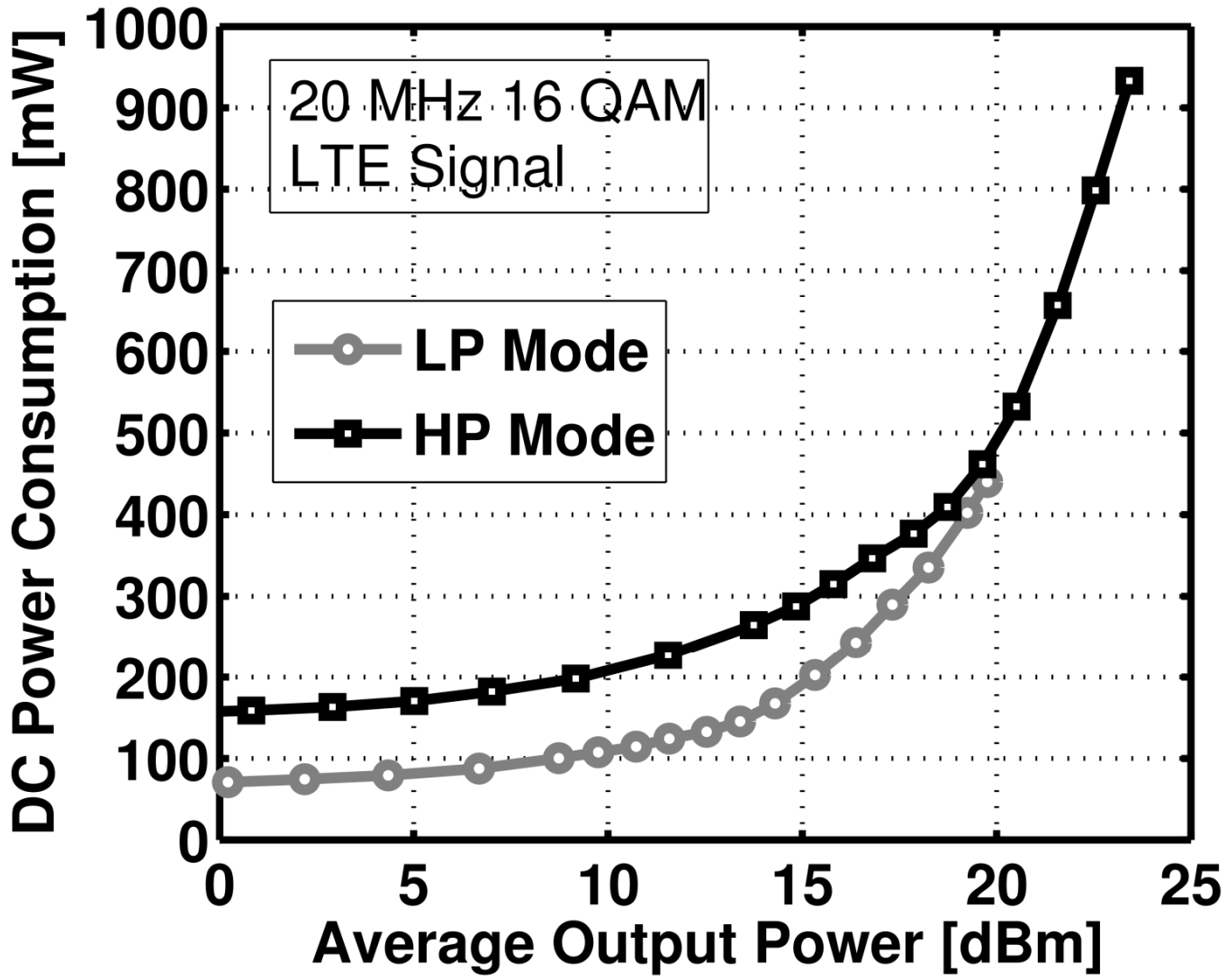
Measurement Results- LTE (2)

- 20 MHz 16 QAM LTE signal at 1.9 GHz
  - HP Mode: 23.4 dBm output power with 23.3 % PAE
  - LP Mode: 19.8 dBm output power with 21.1 % PAE





Measurement Results- LTE (3)



Comparison- LTE Power Amplifiers

	Gain [dB]	P_{MAX}# [dBm]	PAE@ P_{MAX} [%]	PAE@ P_{MAX}-6 dB [%]	PAE@ P_{MAX}-12 dB [%]	Fully Integrated?	Technology, Supply [V]	Technique
C.Yunsung [MTT13]	24 /11*	27	37	22	21*	No	180nm CMOS + InGaP/GaAs,3.4V	dual mode envelope tracking (dual chip)
R. Wu [JSSC13]	17	27.9	40.2	20	10	No	0.35µm BCD + 0.35µm SiGe, 5V	envelope tracking (dual chip)
L. Yan Li [MTT11]	17	24.3	42	18	6	No	0.35µm SiGe BiCMOS,4.2V	envelope tracking
K.Onizuka [ISSCC13]	12	21.3	18	13*	5*	Yes	65nm CMOS, 3.3V	envelope tracking
This work	**21.3 /18.2***	**23.4**	**23.3**	**18.4***	**11.1***	**Yes**	**40 nm CMOS,1.5V**	**Doherty + Mode Switching**

P_{MAX} is defined as the measured average output power for which the ACLR1, ACLR2 and EVM specs are met.
* Low Power (LP) Mode

Conclusion

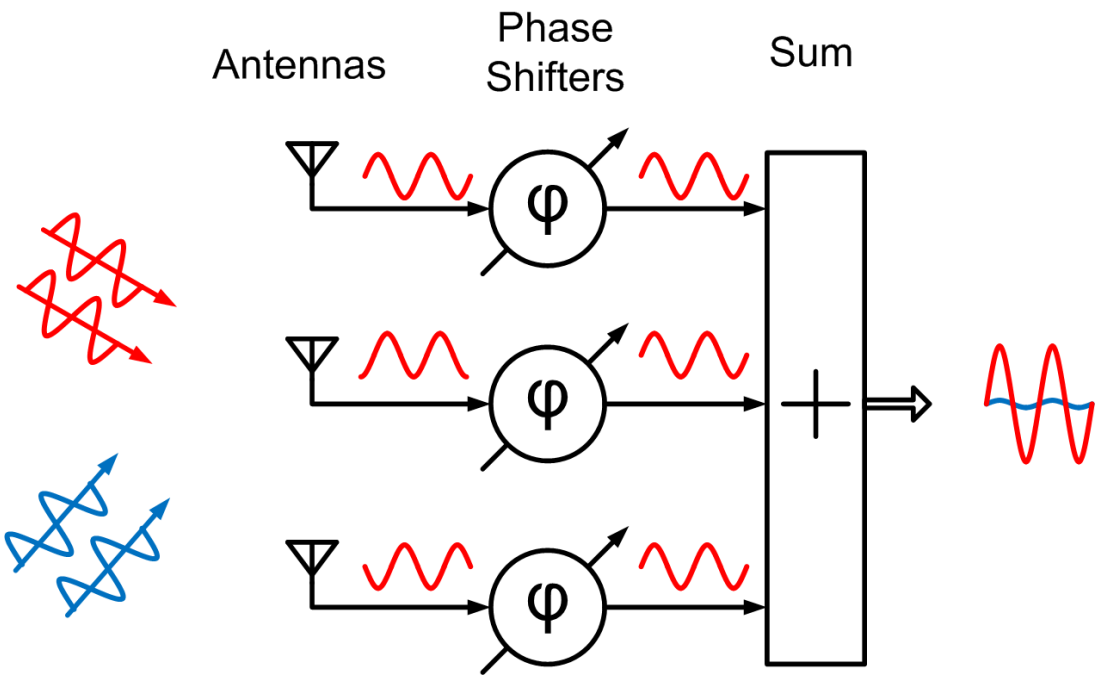
- This PA combines two efficiency enhancement techniques
  - Doherty + Mode Switching
- 4 push-pull amplifiers to achieve high output power
- High efficiency with 20 MHz LTE signal

A 1.0-to-2.5GHz Beamforming Receiver with Constant-G_m Vector Modulator Consuming < 9mW per Antenna Element in 65nm CMOS

Michiel Soer[1], Eric Klumperink[1],
Bram Nauta[1], Frank van Vliet[1,2]

[1] IC-Design Group, University of Twente, The Netherlands
[2] TNO, The Hague, The Netherlands

Beamforming Principle

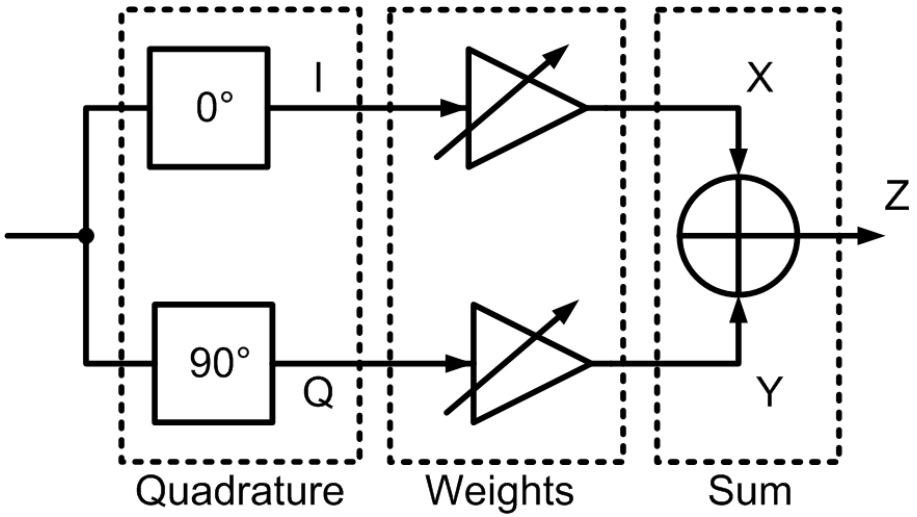


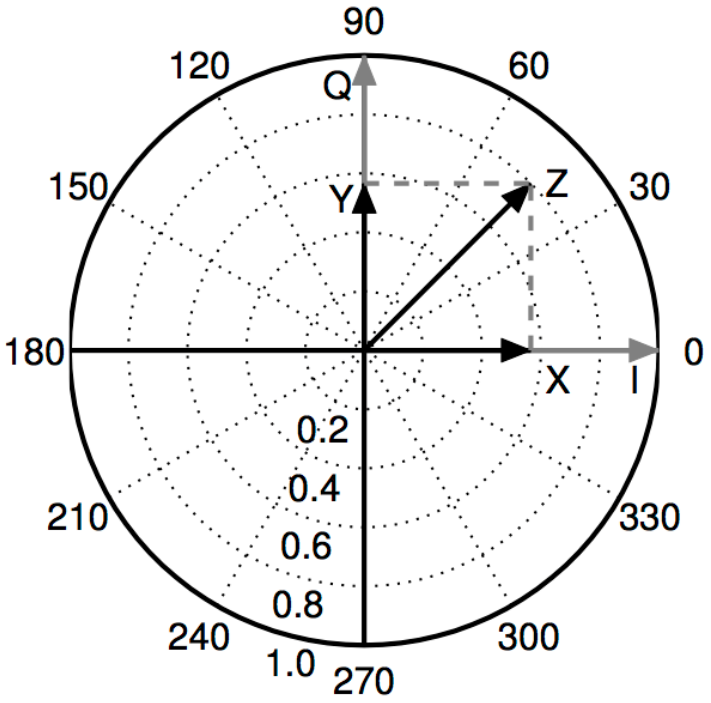
- Benefits over single antenna:
  - Increased sensitivity (3dB / doubling of antennas)
  - Spatial filtering for interference rejection

Challenge: Increased power consumption

Phase Shifter: Vector Modulator

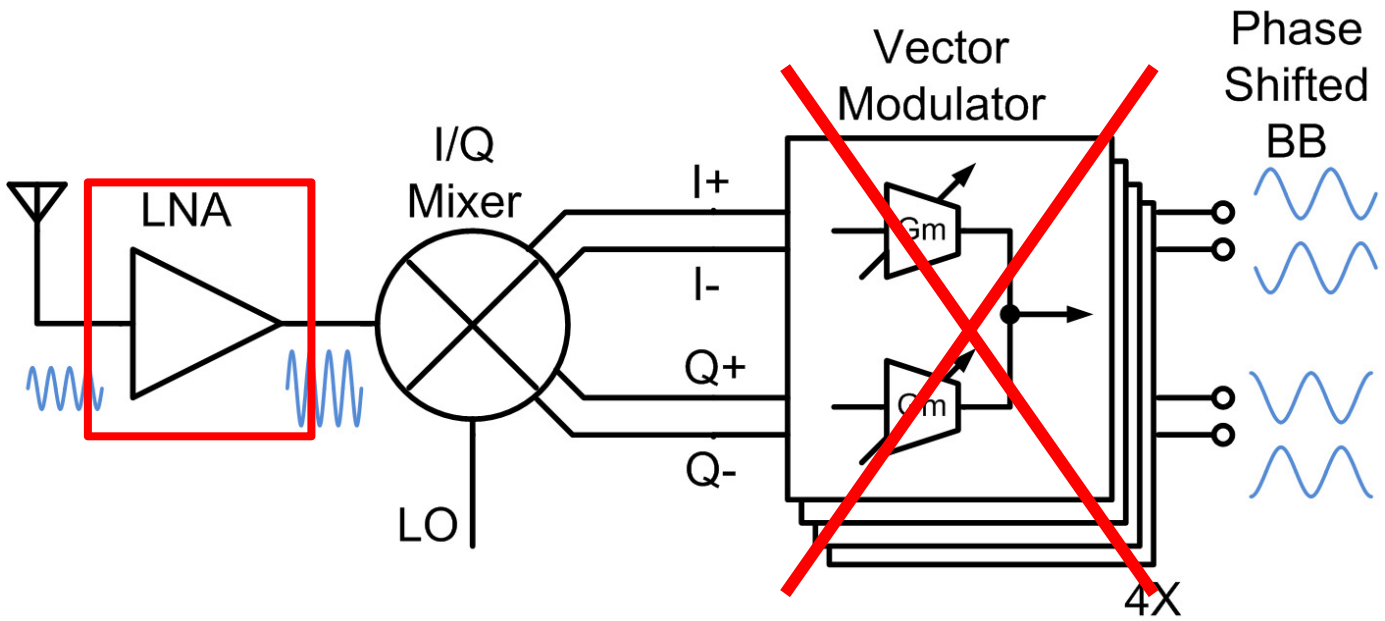
- Interpolate between 90° out-of-phase signals
  - Produce I/Q signals
  - Weight with amplitude/phase weight
  - Sum into phase-shifted signal





Typical Baseband Phase Shifting

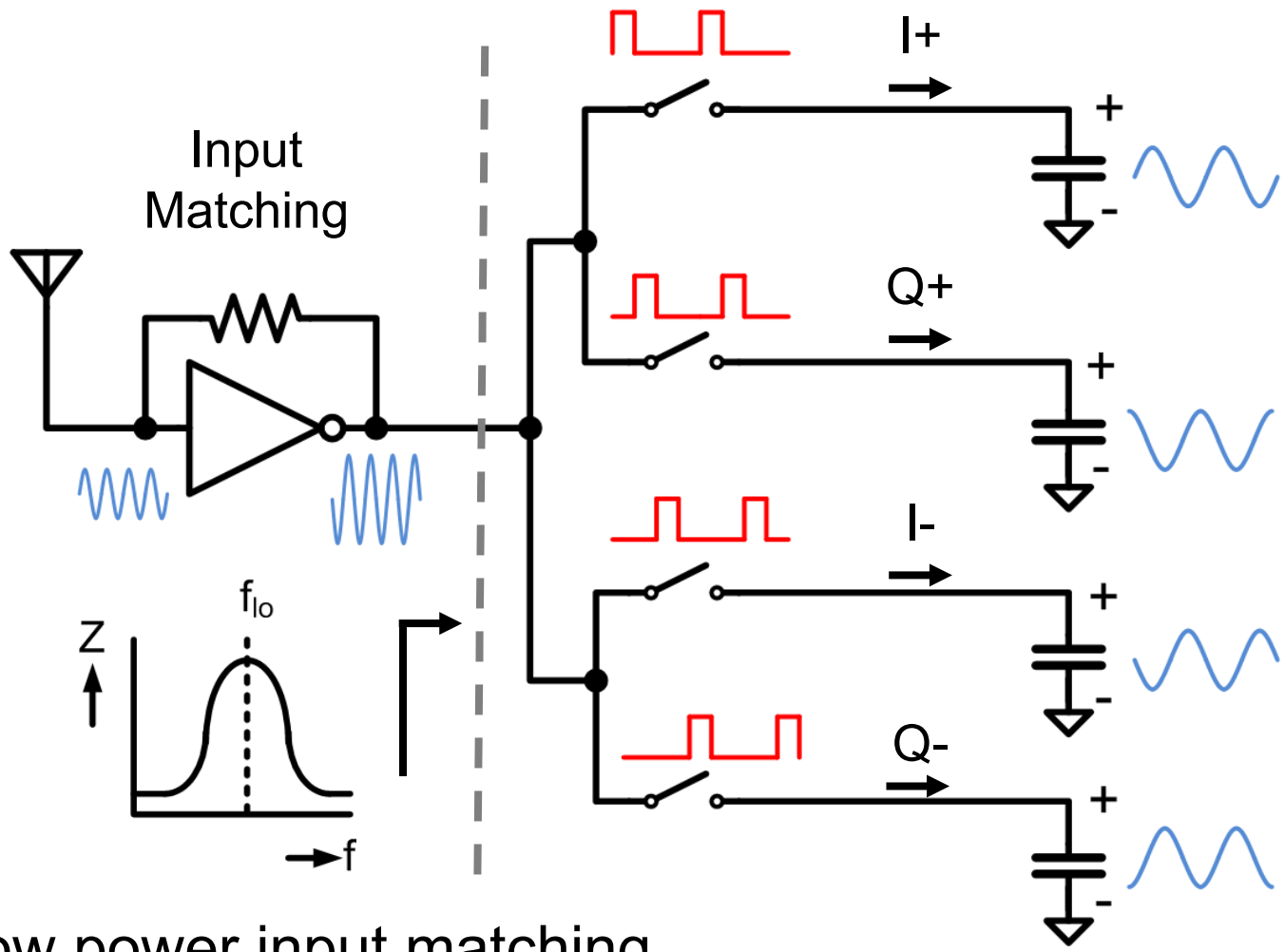
- Mixer as I/Q generator
- ~~Weighting~~ and summing at BB



- 4-phase BB signals ⇨ 4x power consumption

Goal: RF Transconductor + BB Summing

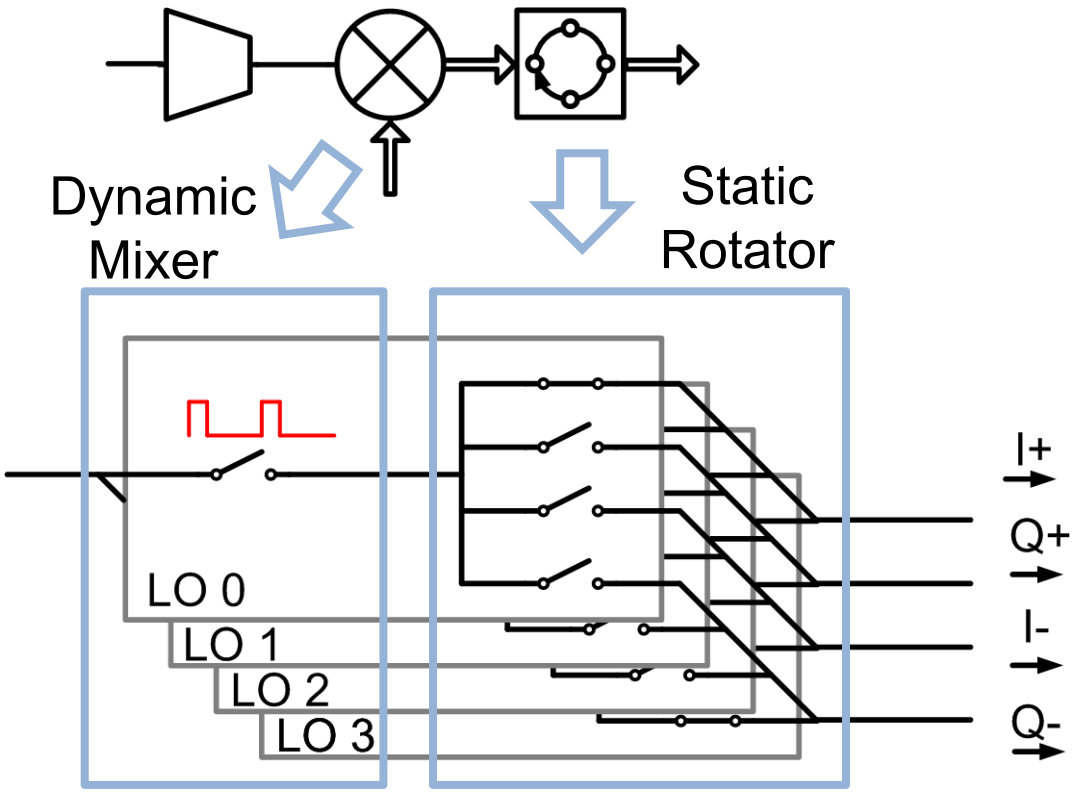
Inverter LNA + Passive Mixer Topology

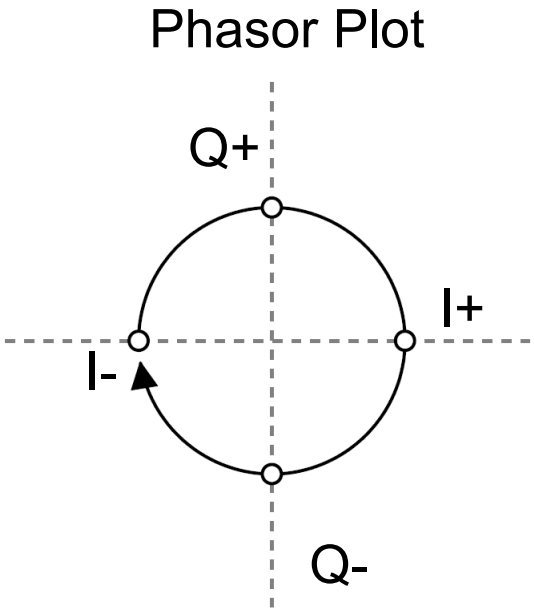


- Low power input matching
- Boosted LNA out-of-band linearity (RLC load)
- LNA current steered to Quadrature outputs

Step 1: Phase Swapping

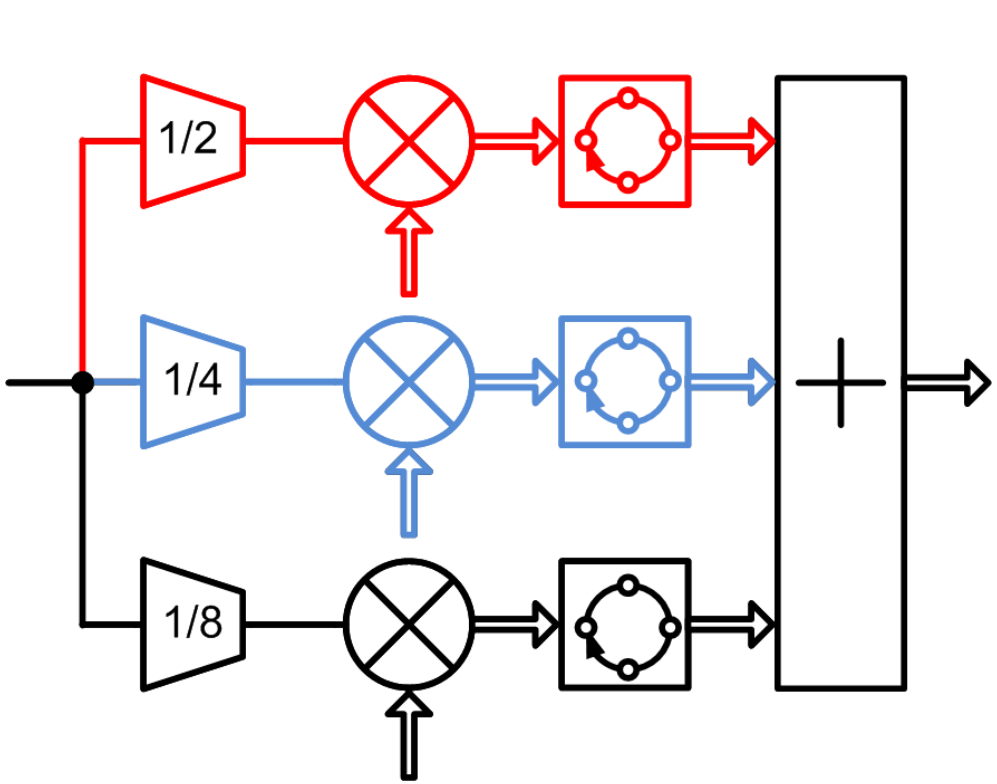
- Add reconfiguration switches to mixer outputs
  - Rotates phases
  - 4-step phase shifter for free

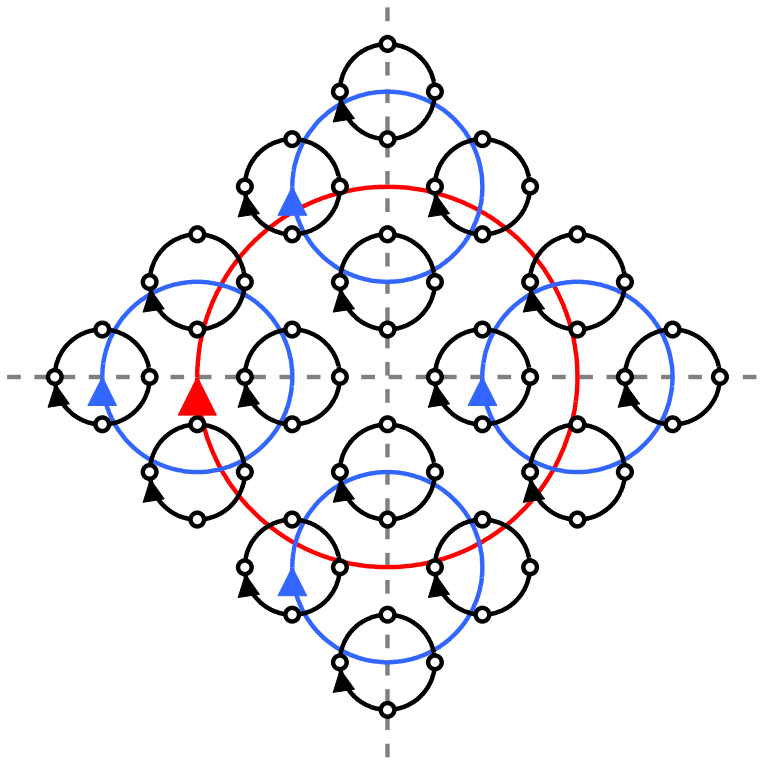




Step 2: Increase Resolution

- Sum currents from binary weighted slices:

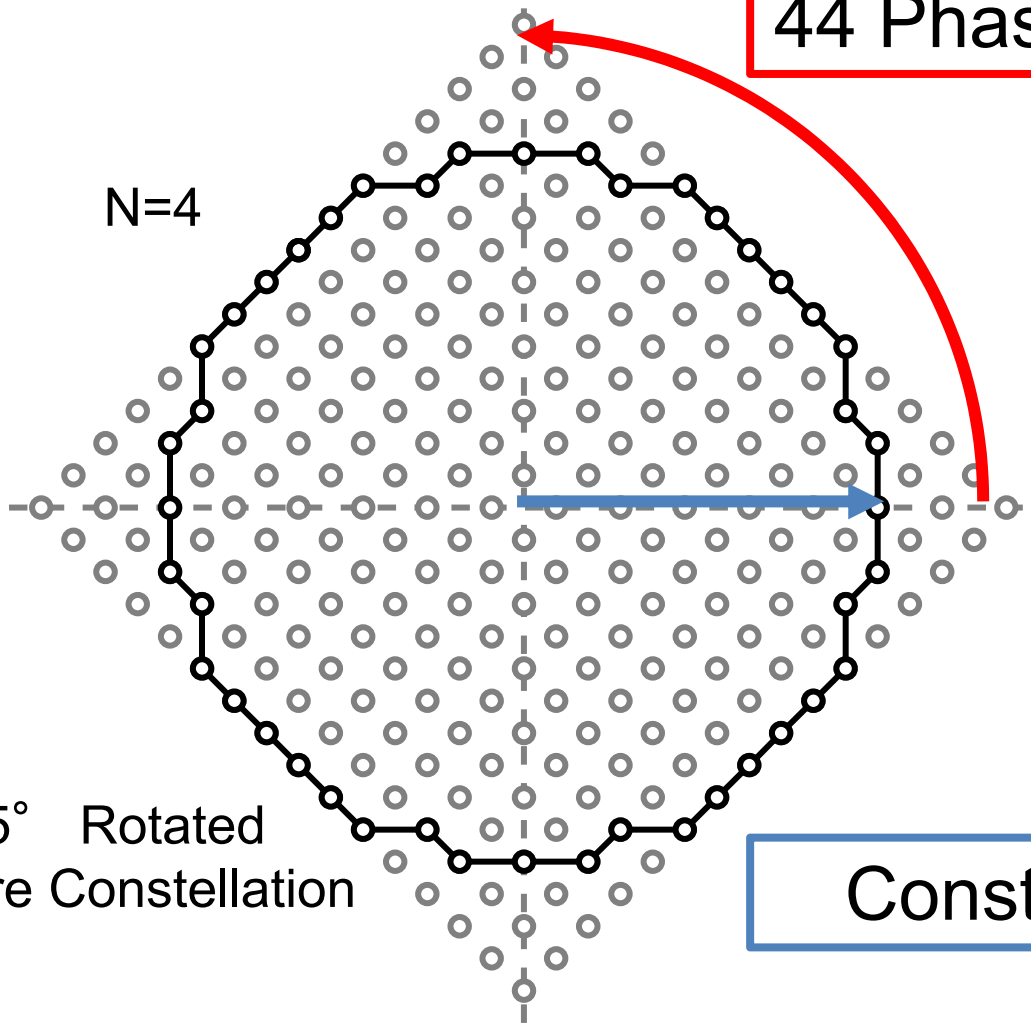




- Resolution improves with #slices
  - N bits = 2^N X 2^N grid

Step 3: Map Constellation to Phase Shift

44 Phase steps (8.2°)

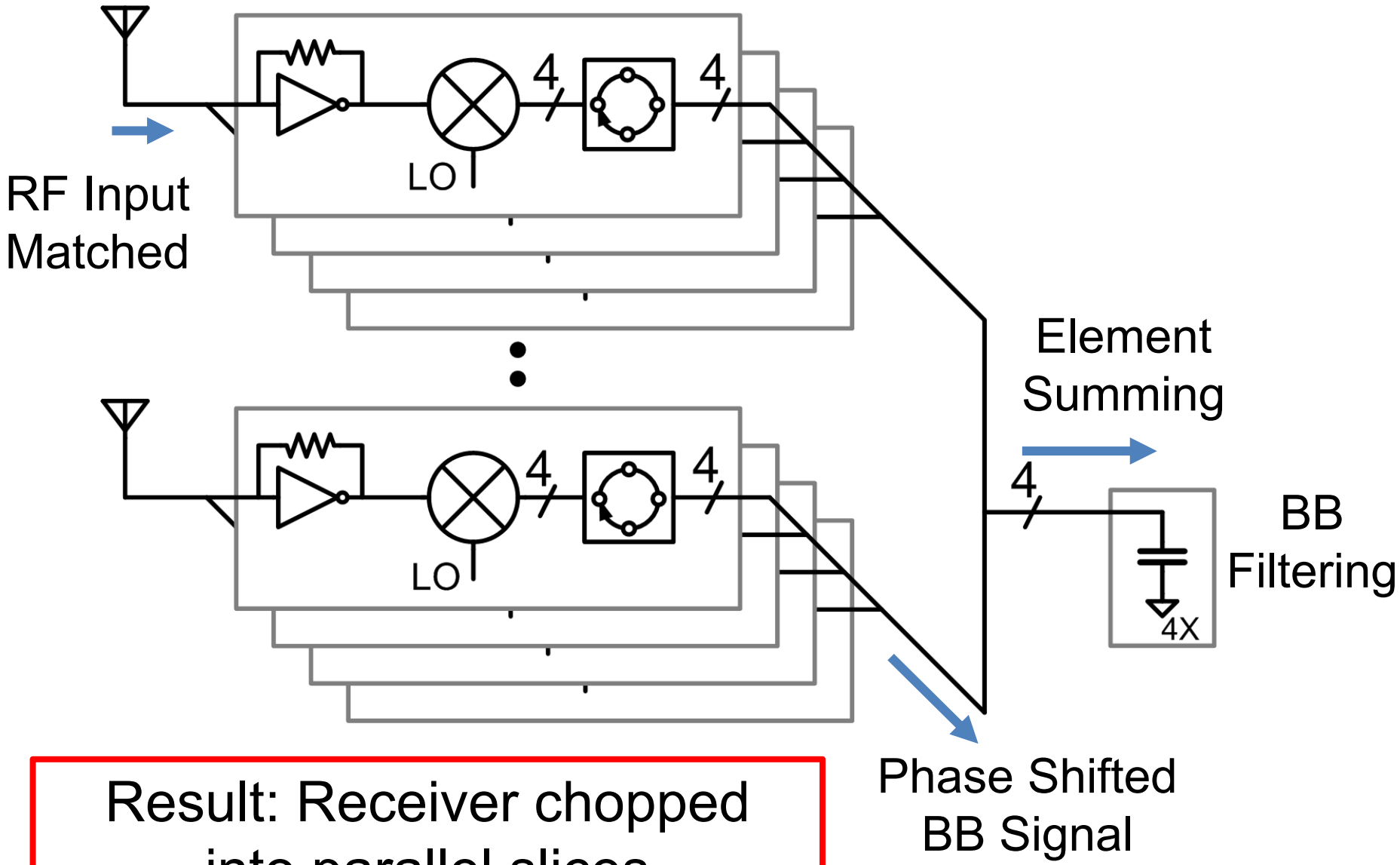


45° Rotated
Square Constellation

Constant amplitude

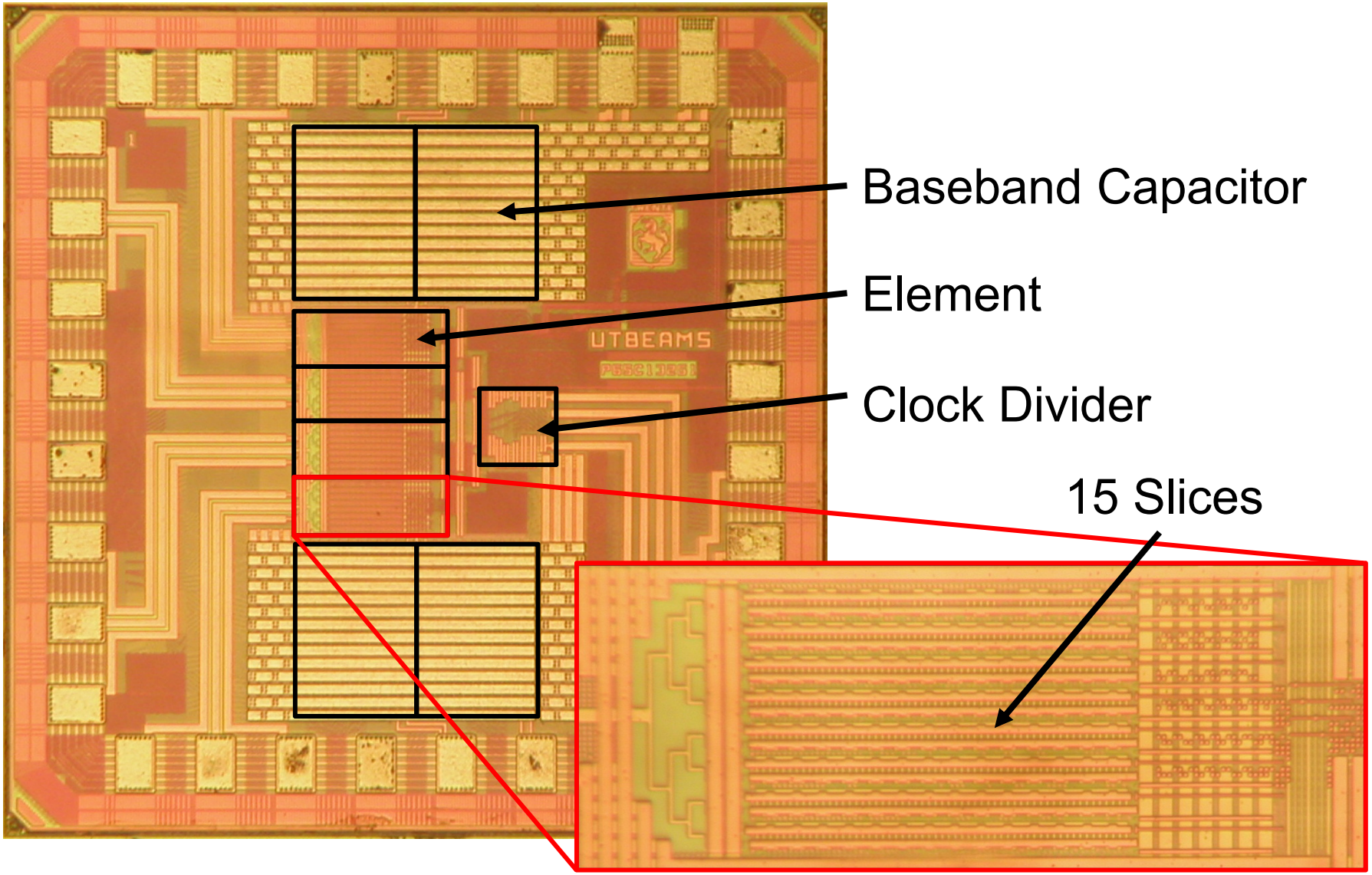
(Identical to conventional vector modulator)

Constant-Gm Beamforming Architecture



Result: Receiver chopped into parallel slices

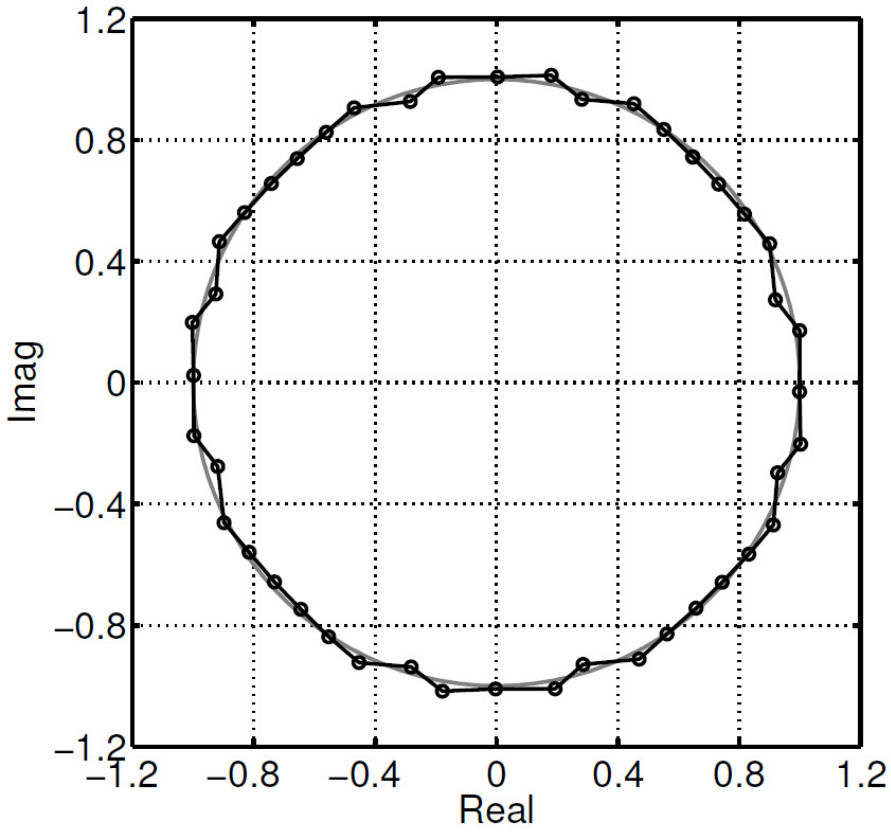
Chip Photograph



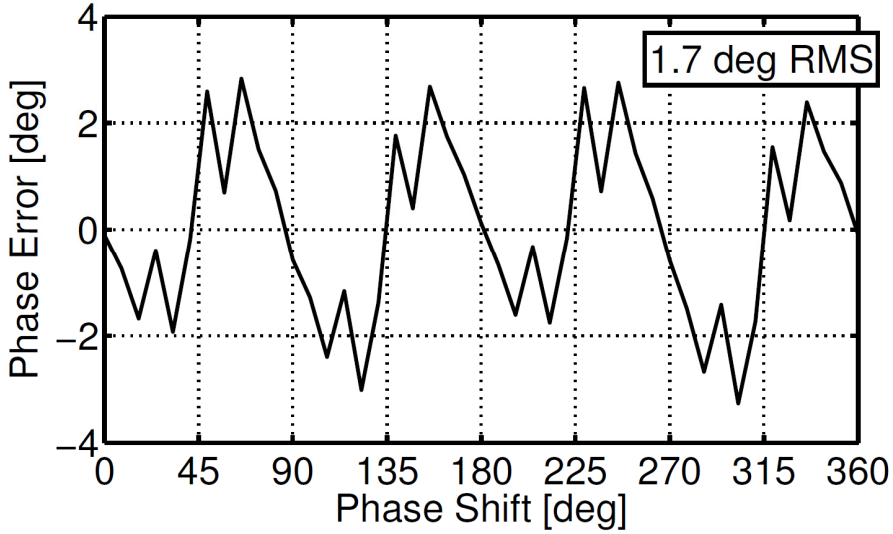
65nm LP CMOS, 0.2mm^2 active area

Measured: Phase Shifter

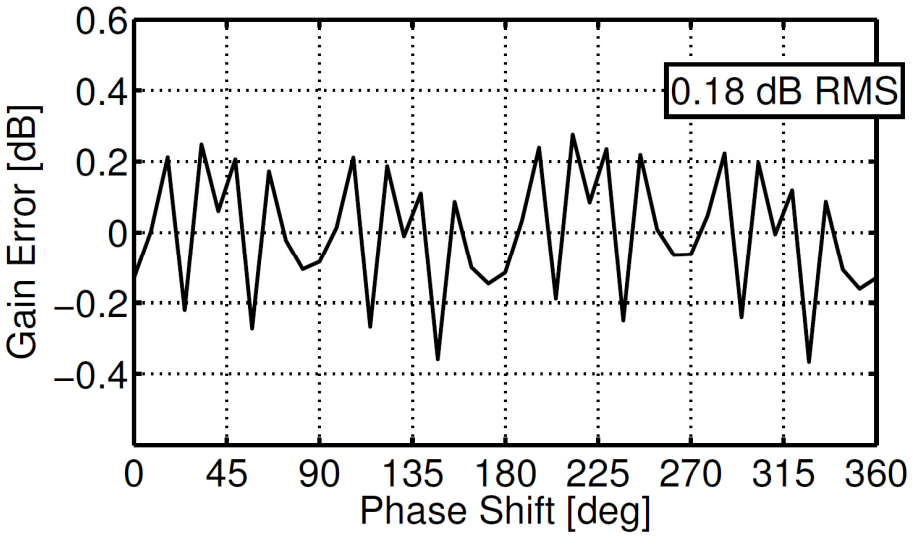
Phasor Plot



Phase Error



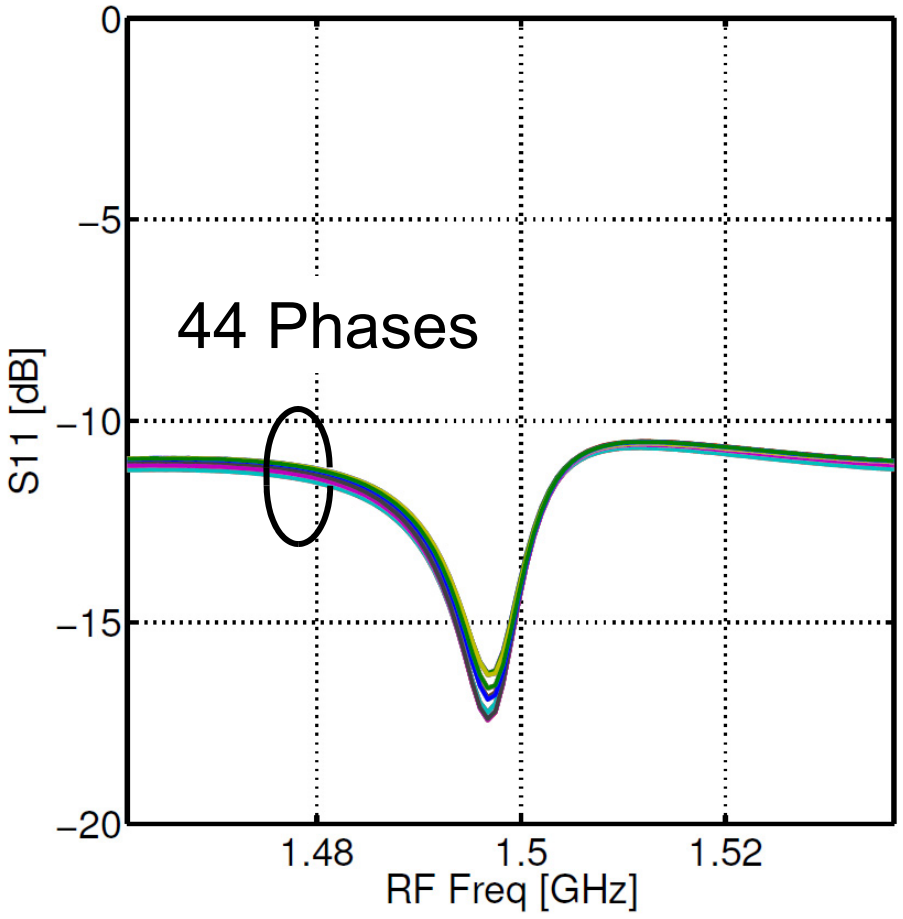
Gain Error



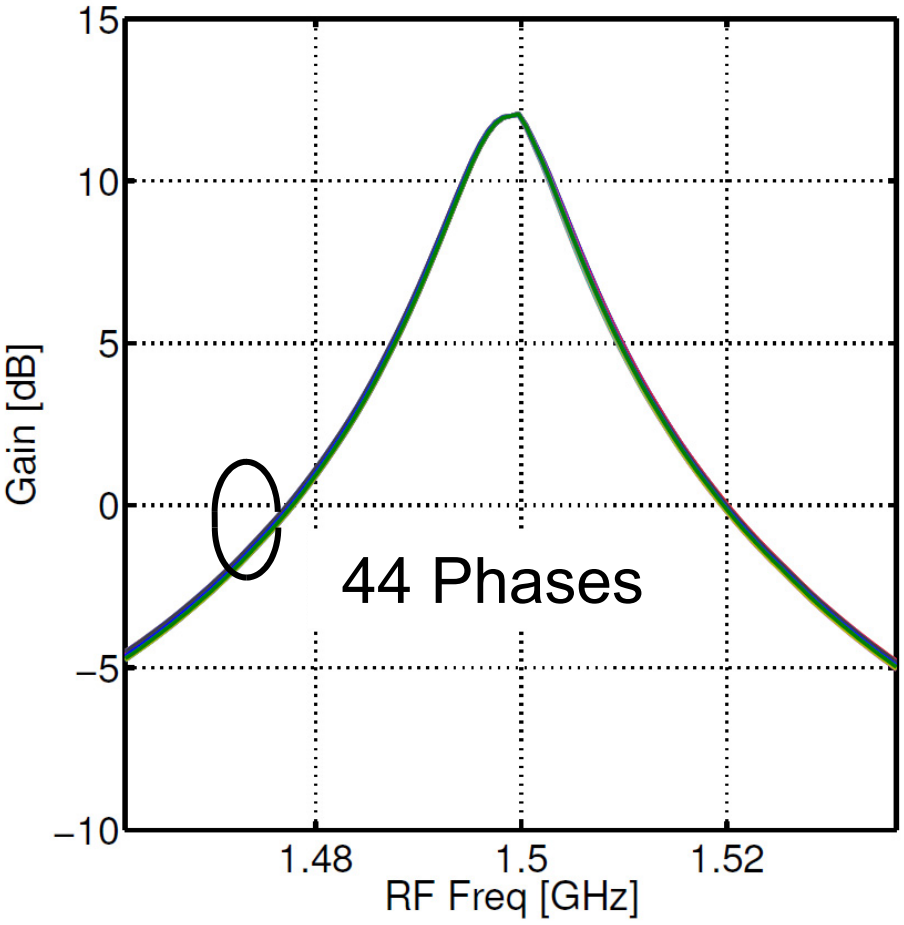
1.7° and 0.18 dB RMS Error

Measured: S11 and Gain

Impedance Match

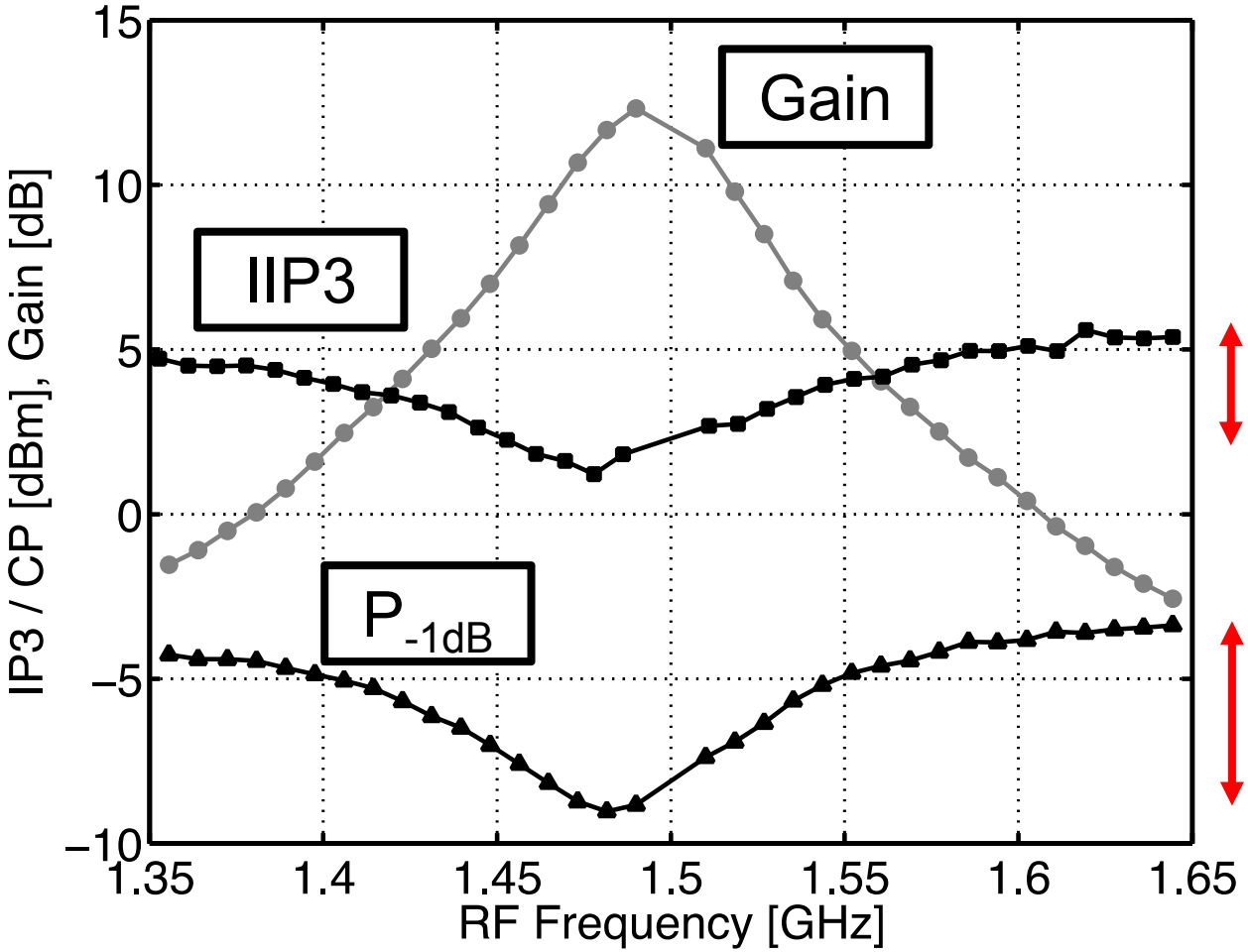


Bandwidth



Code independent due to constant G_m

Measured: Linearity

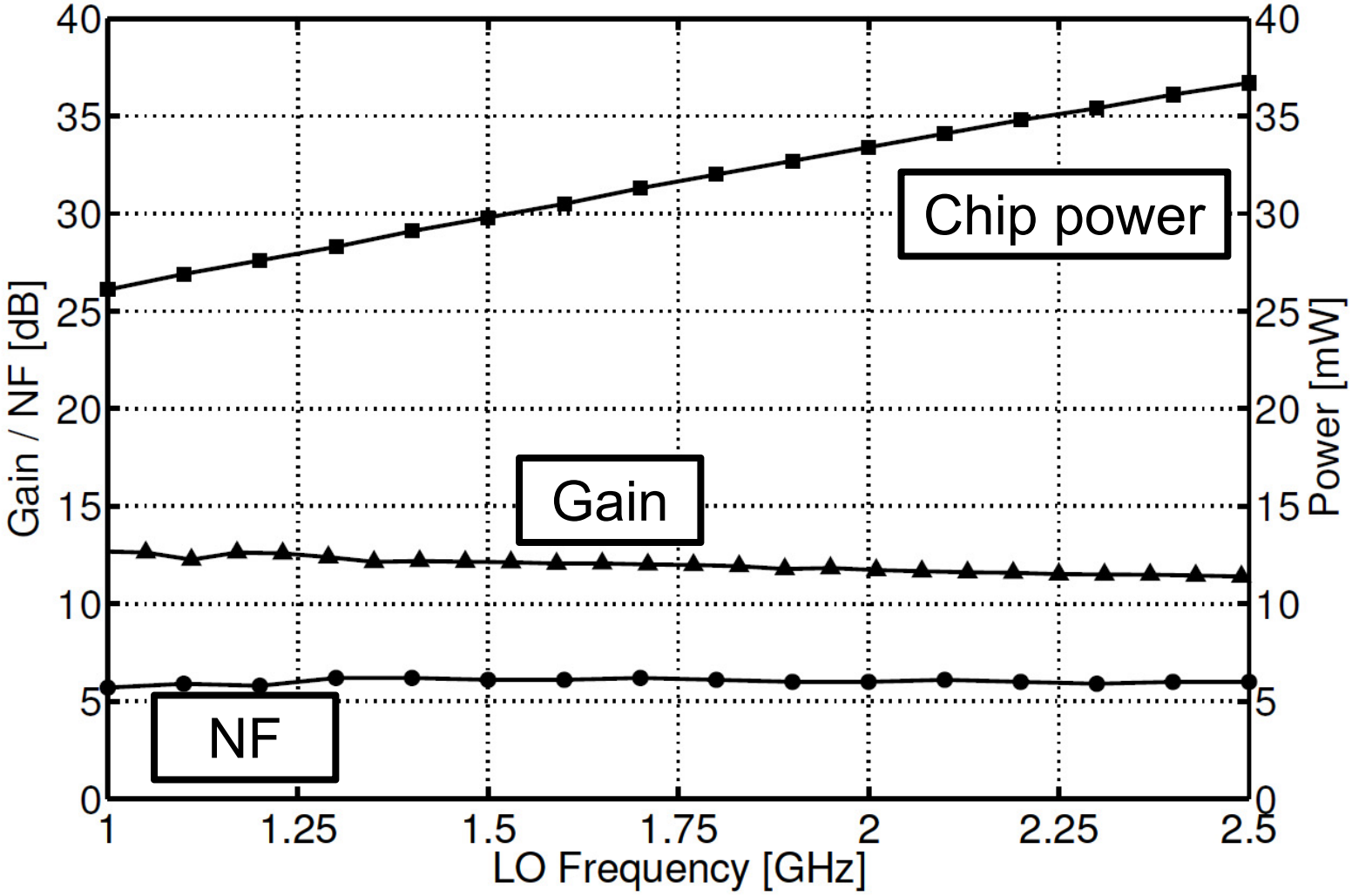


1 to 5 dBm IIP3

-9 to -3 dBm Compression Point

Mixer load on inverter boosts out-of-band linearity

Measured: Power, Gain, NF



Power Consumption: < 9mW per Element

Performance Summary

		Tseng, JSSC2010	Soer, ISSCC2012	Ghaffari, ISSCC2013	This Work	
Technology		90nm	65nm	65nm	65nm	
Active area		1.4 [a]	0.18	0.97	0.20	mm^2
Supply voltage		1.2	1.0 - 1.2	1.2	1.0	V
RF frequency band		4.0	1.5 – 5.0	0.6 - 3.6	1.0 – 2.5	GHz
Single element performance:						
Power per element		41	16 – 42	17 - 49	6.5 - 9	mW
Gain		15	-6	-1	12	dB
Noise figure		13	18	4 [b]	6	dB
In-band SFDR in 1MHz BW		69	73	77	73	dB
Compression point	In-band	N/A	2	-5	-9	dBm
IIP3	In-band	2	13	6	1	dBm
# Phase shifter steps		32	32	8	44	

[a] Estimated from chip photograph.

[b] Degraded by 2dB for 4 elements, due to correlated noise.

Conclusions

- Baseband phase shifting with constant-G_m modulator:
  - Power saved by removing baseband G_ms
  - LNA + mixer chopped into binary-weighted rotator slices
  - Code-independent input matching and bandwidth

- Low power phased array receiver implemented:
  - 44 phase shifter steps, 1.7° and 0.18dB RMS error
  - State-of-the-art spurious free dynamic range
  - 6dB element NF
  - < 9mW / element power consumption

Acknowledgments

STMicroelectronics for silicon donation

CMP for their assistance

Gerard Wienk and Henk de Vries for technical support

Thank you for your attention

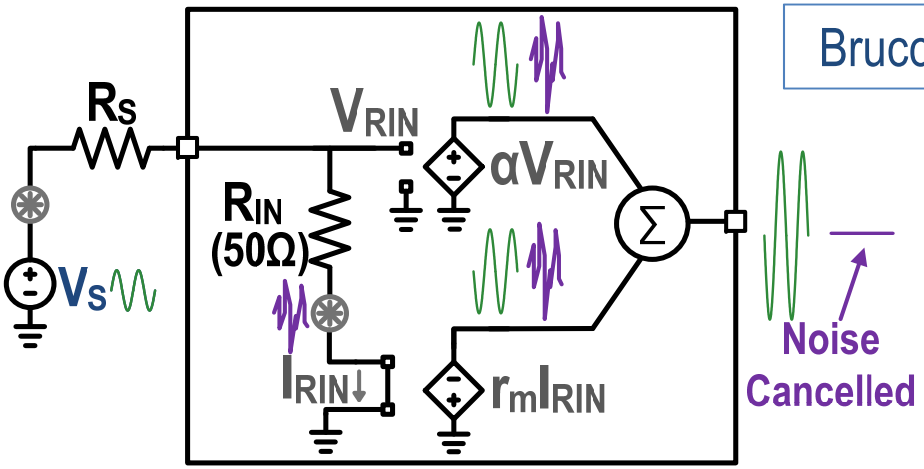
Broadcom Corporation, Irvine, CA

A Noise-Cancelling Receiver with Enhanced Resilience to Harmonic Blockers

David Murphy, Hooman Darabi, Hao Xu

2/10/2014

Noise-Cancelling Receiver

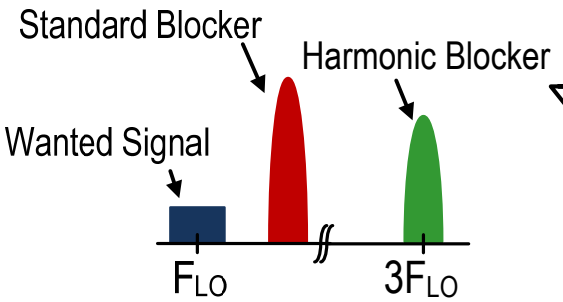


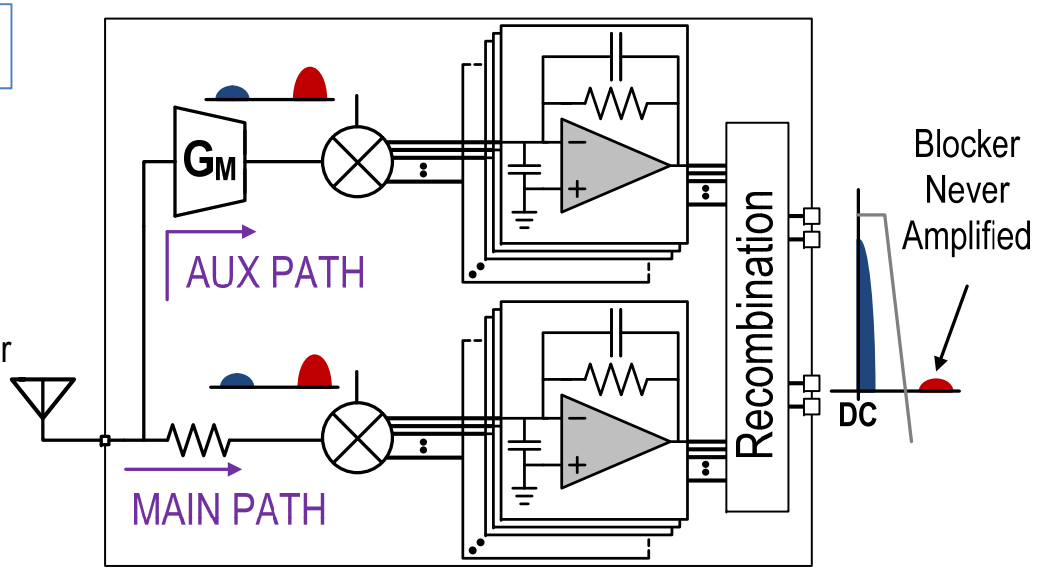
Bruccoleri et. al., ISSCC 2002

UCLA/Broadcom, ISSCC 2012

→ NF = 2dB

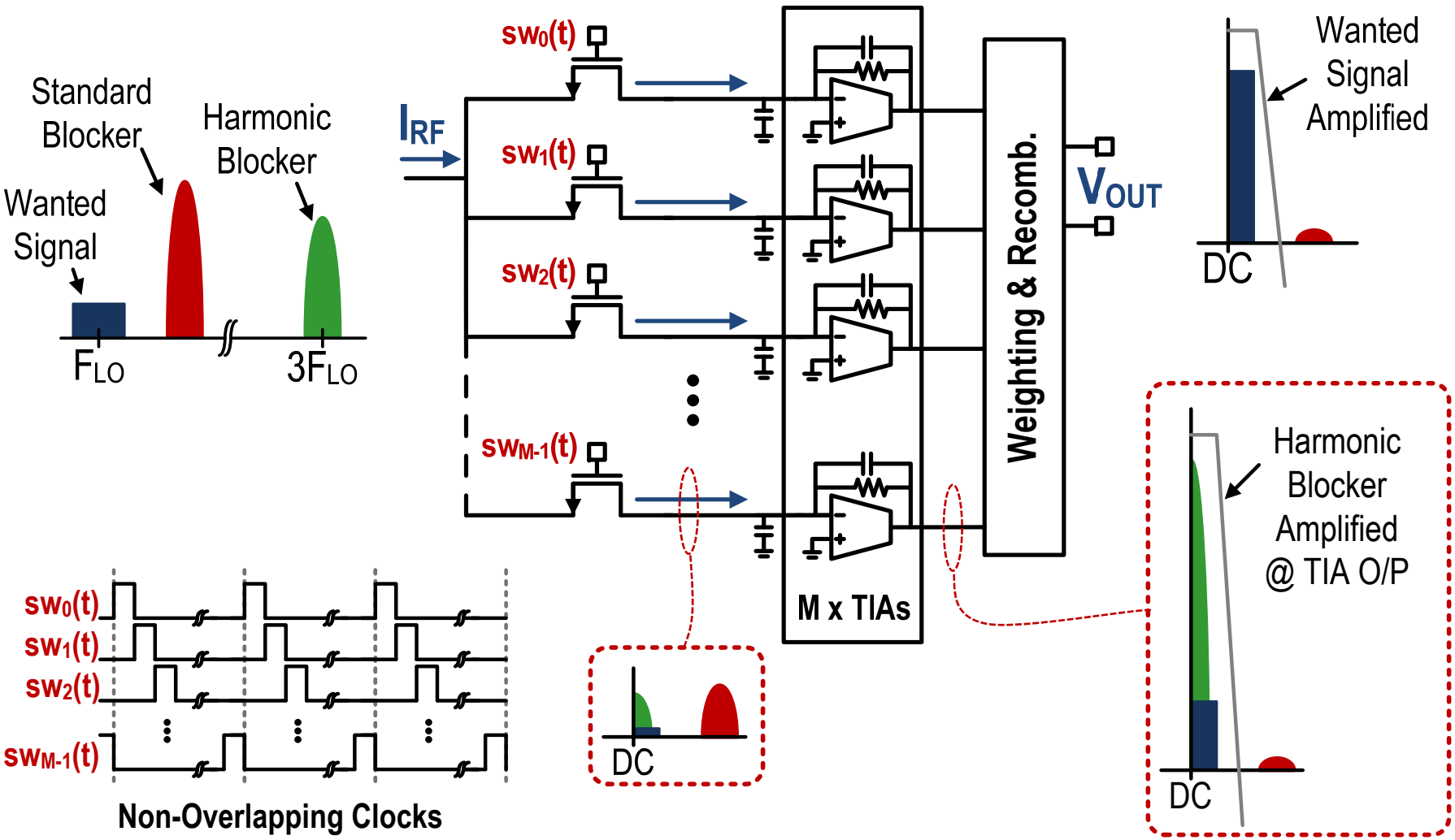
→ 0dBm Blocker NF = 4dB



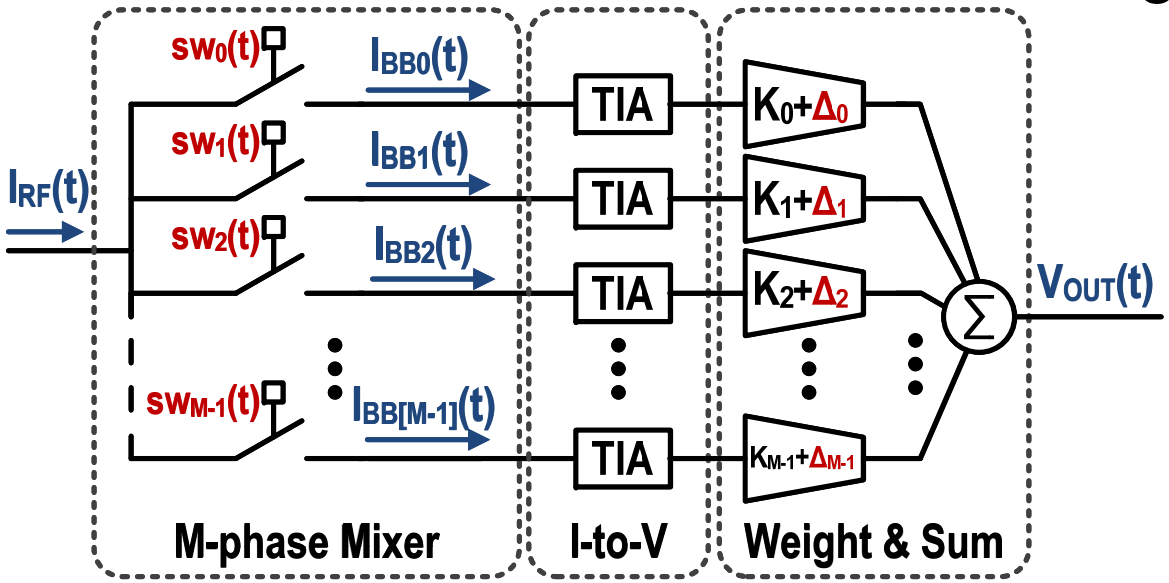


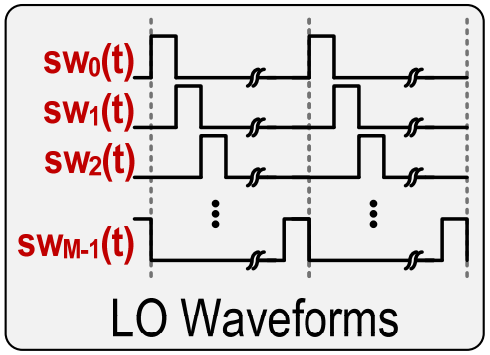
Harmonic blockers → blockers "around" integer multiples of LO frequency

Harmonic Blocker Challenge (1/3)



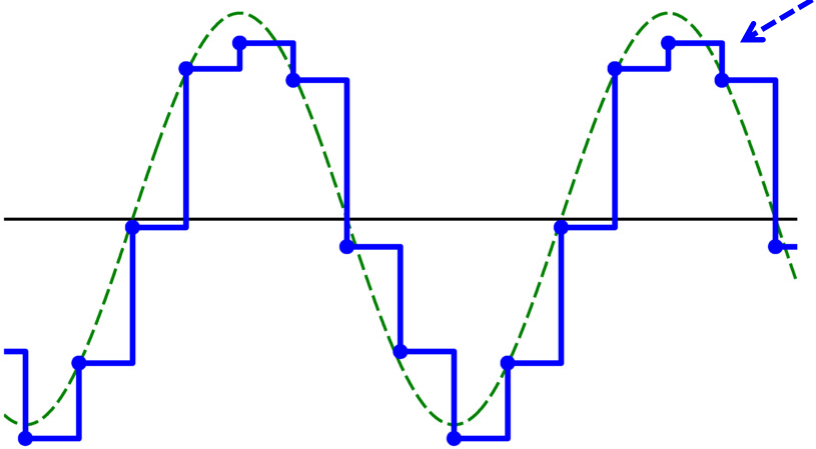
Harmonic Blocker Challenge (2/3)

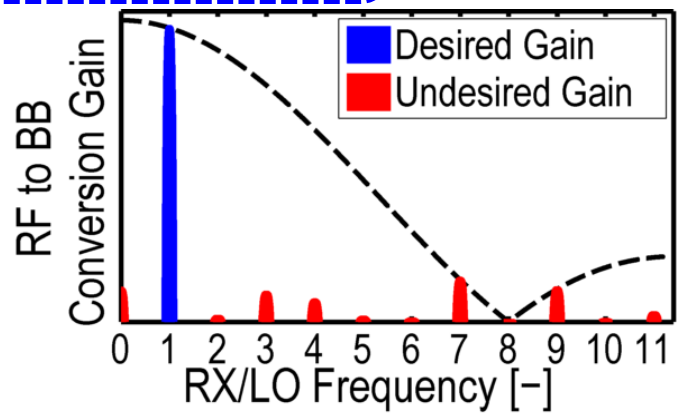




$$v_{OUT}(t) = i_{RF}(t) \sum_{x=0}^{M-1} Z_{TIA} K_x sw_x(t)$$

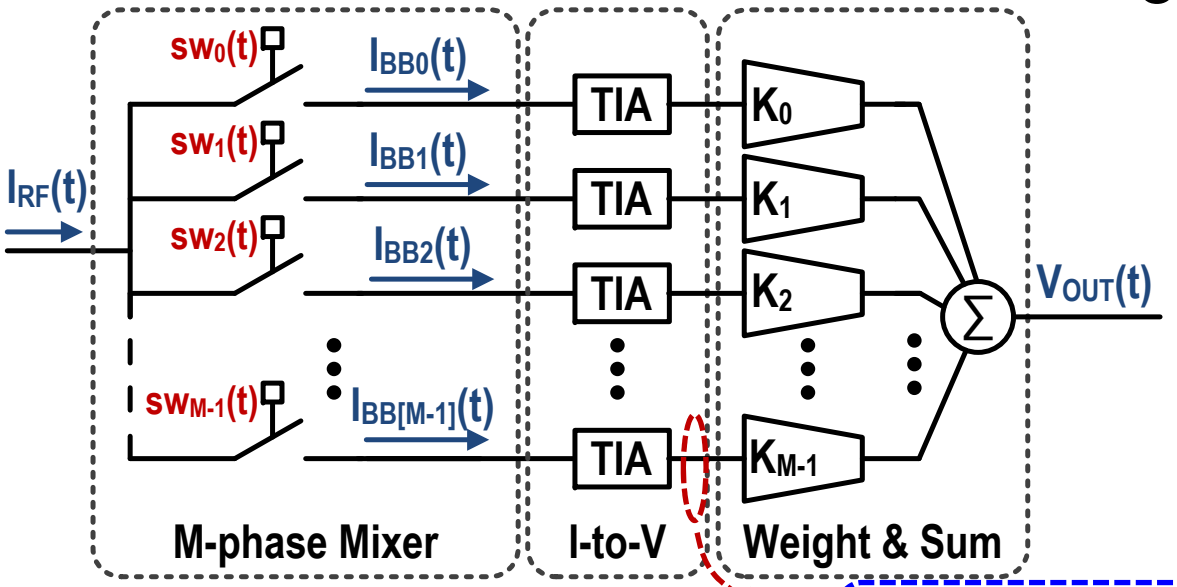
Effective LO

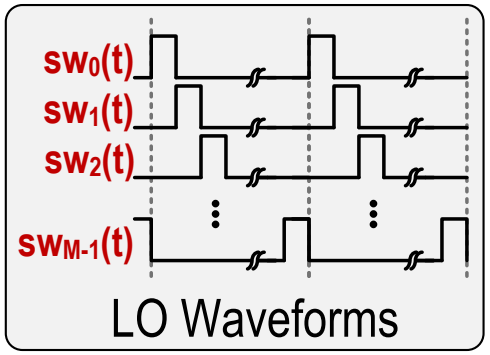




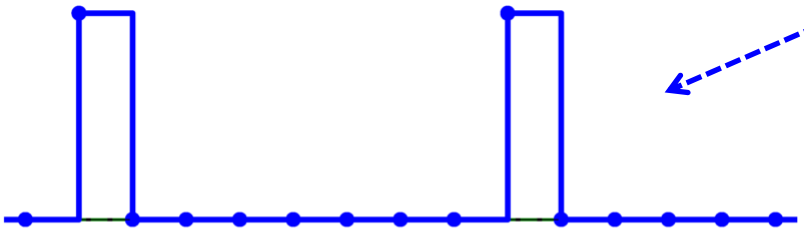
Correct Weighting Constants → Improved Small-Signal Harmonic-Rejection

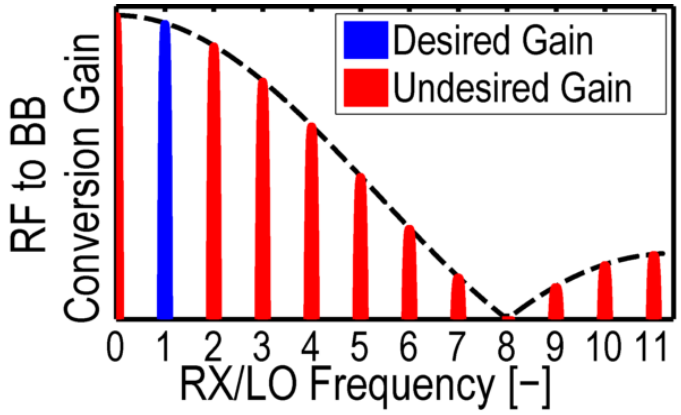
Harmonic Blocker Challenge (3/3)





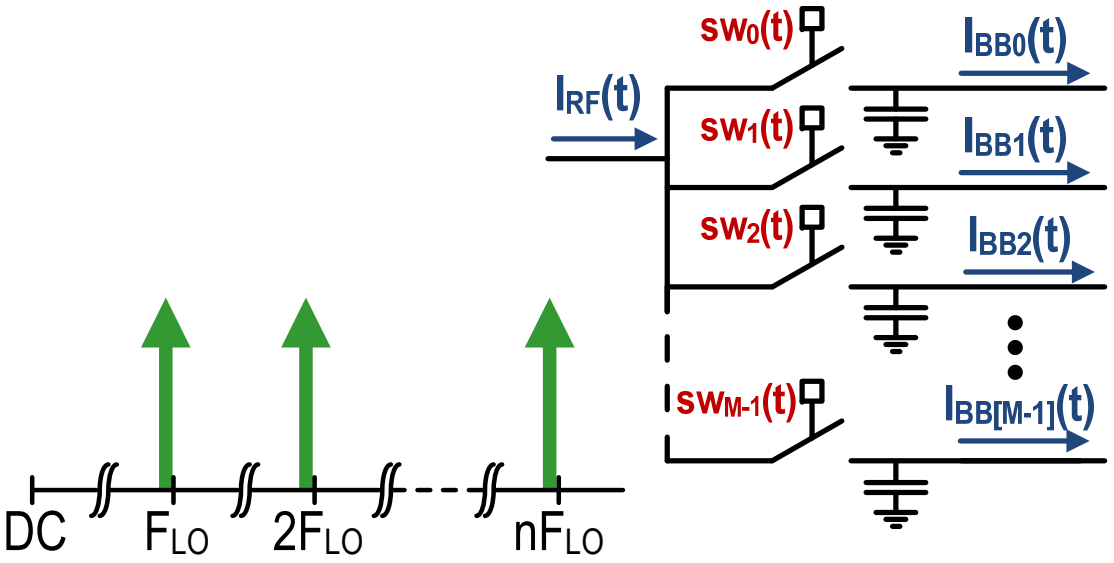
$$v_{TIA_x}(t) = i_{RF}(t) Z_{TIA} sw_x(t)$$ Effective LO

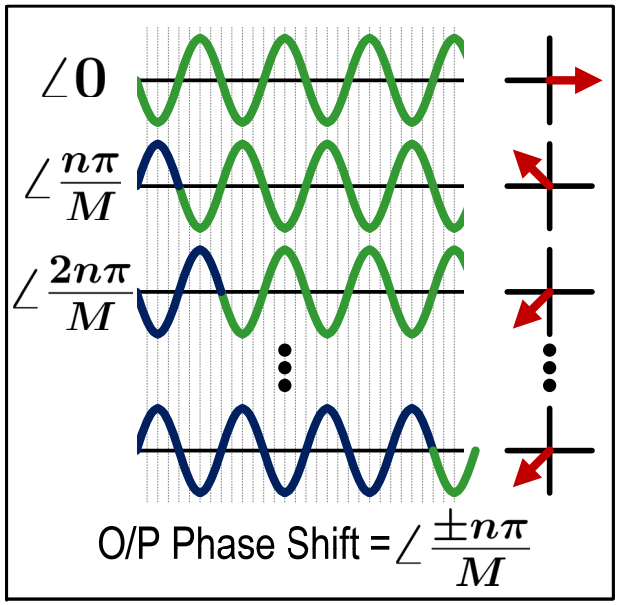


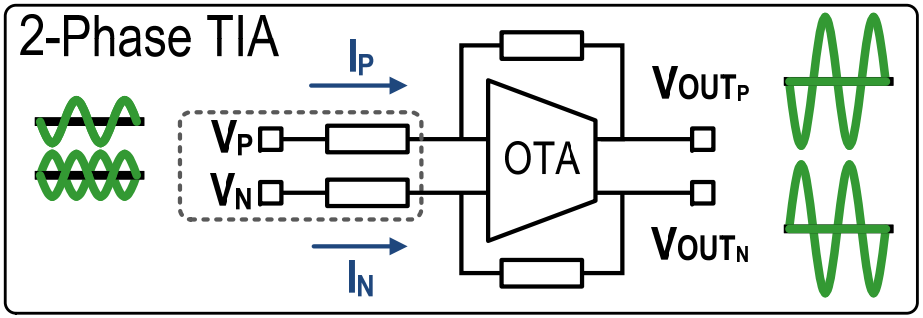


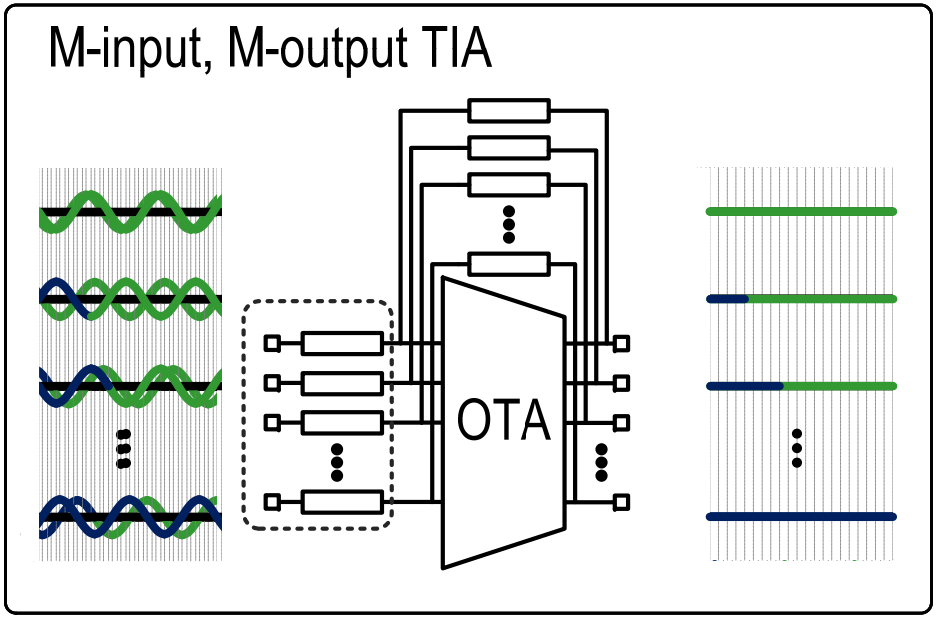
Large-Signal, Harmonic-Blocker Tolerance
→ Avoid Harmonic Gain at TIA o/p

Technique 1: Harmonic Rejection TIAs (1/5)

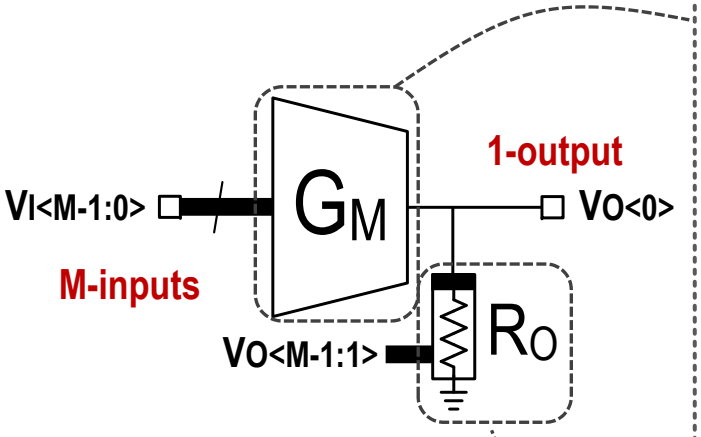


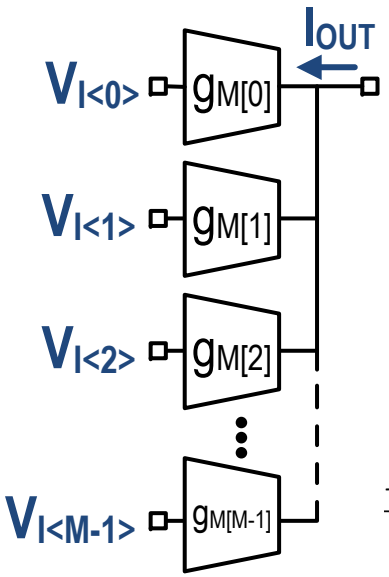


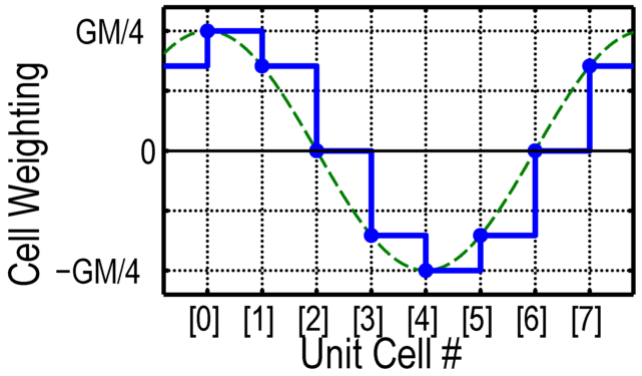




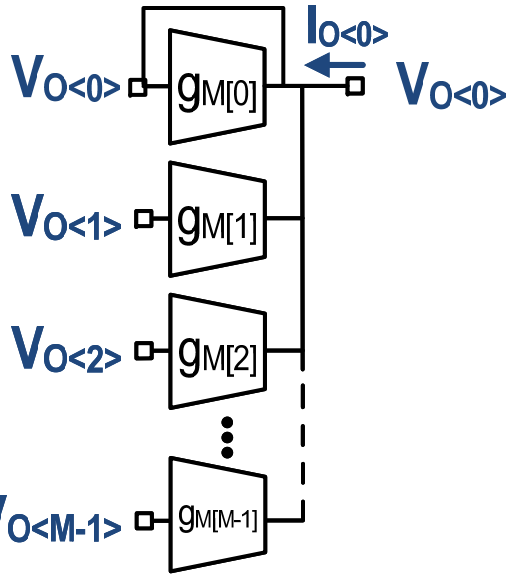
Technique 1: Harmonic Rejection TIAs (2/5)

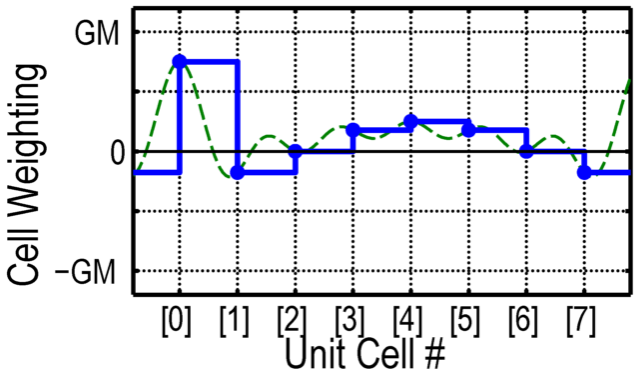




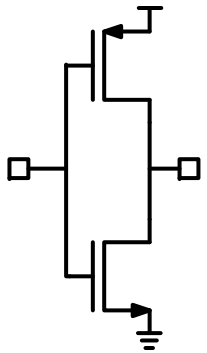


$$\frac{I_{OUT}}{|V_I|} \approx \begin{cases} G_M, & \text{if } \Delta\theta = \pm\pi/M \\ 0, & \text{otherwise} \end{cases}$$



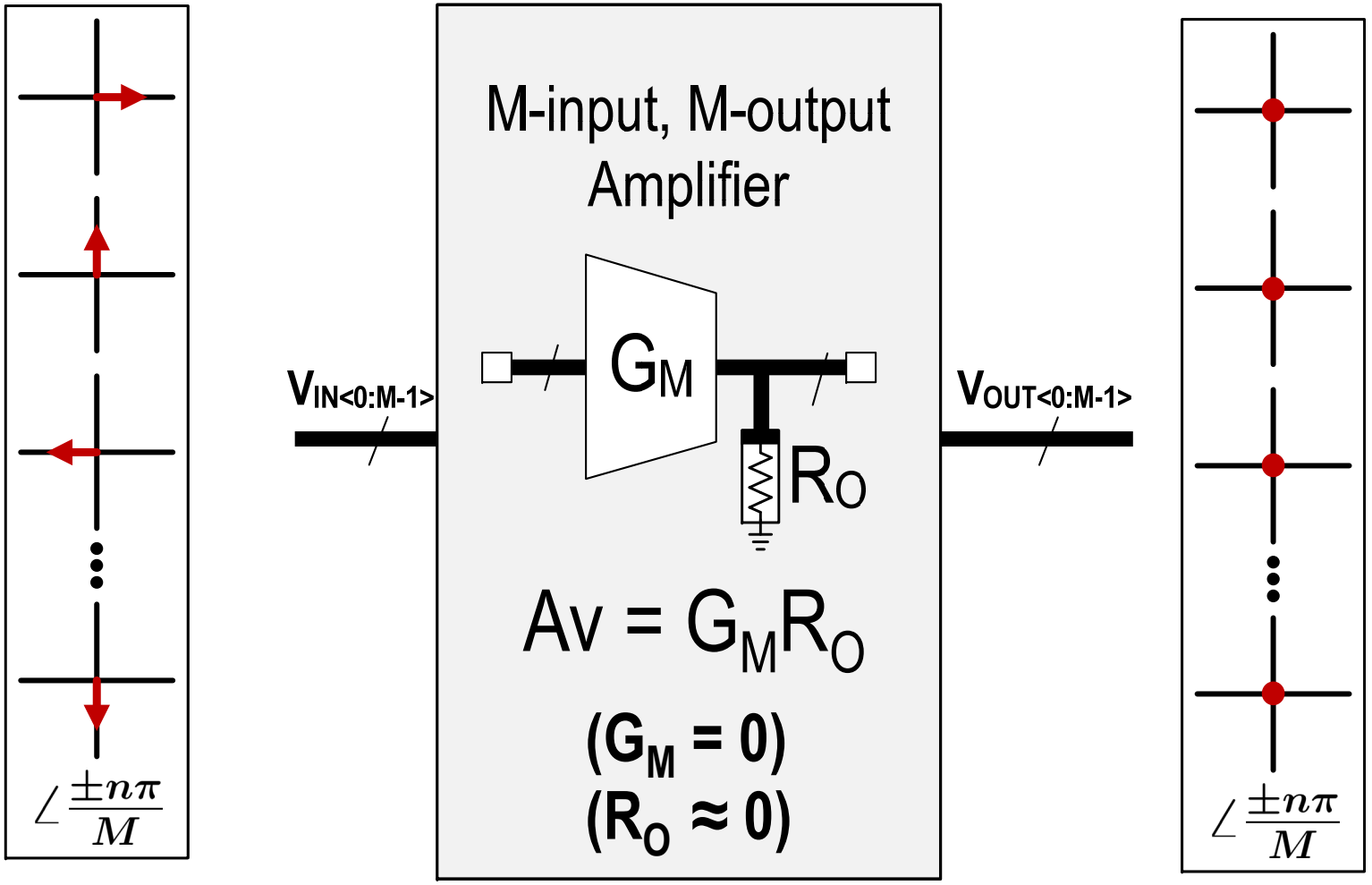


$$R_O \approx \begin{cases} \infty, & \text{if } \Delta\theta = \pm\pi/M \\ 1/G_M, & \text{otherwise} \end{cases}$$



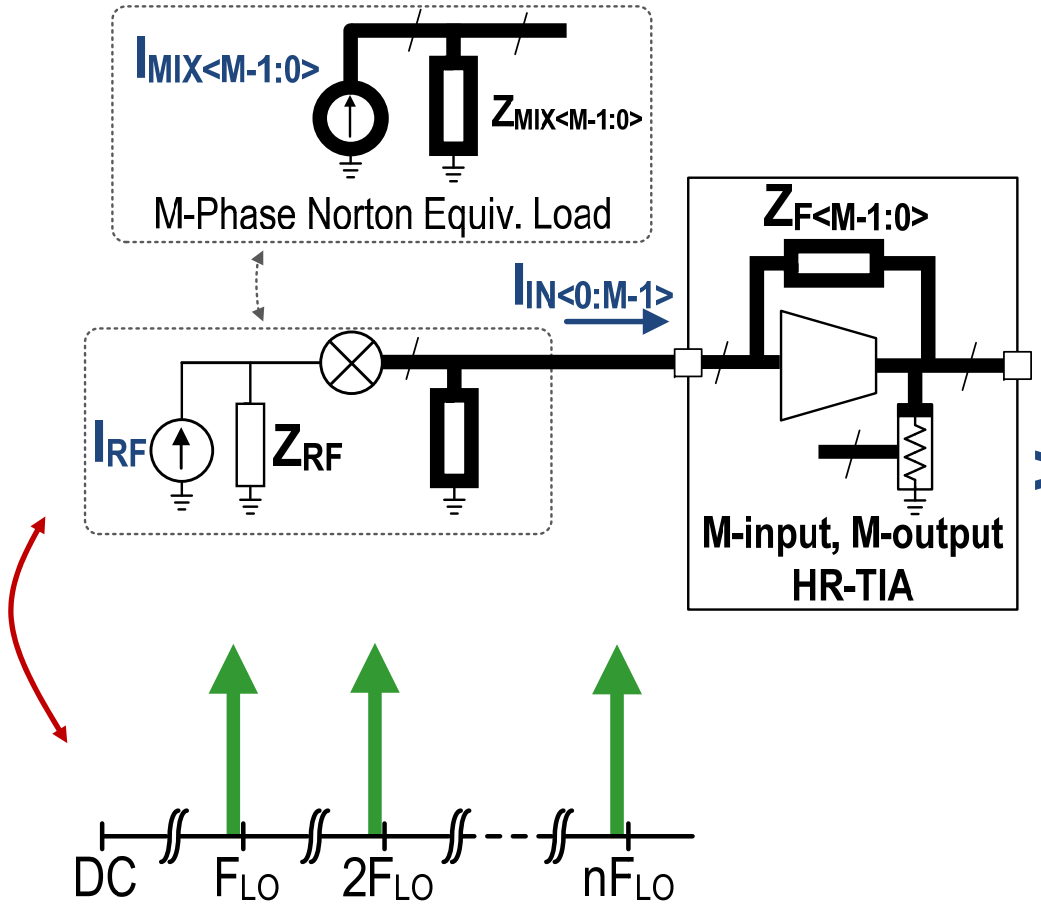
gM Unit Cell

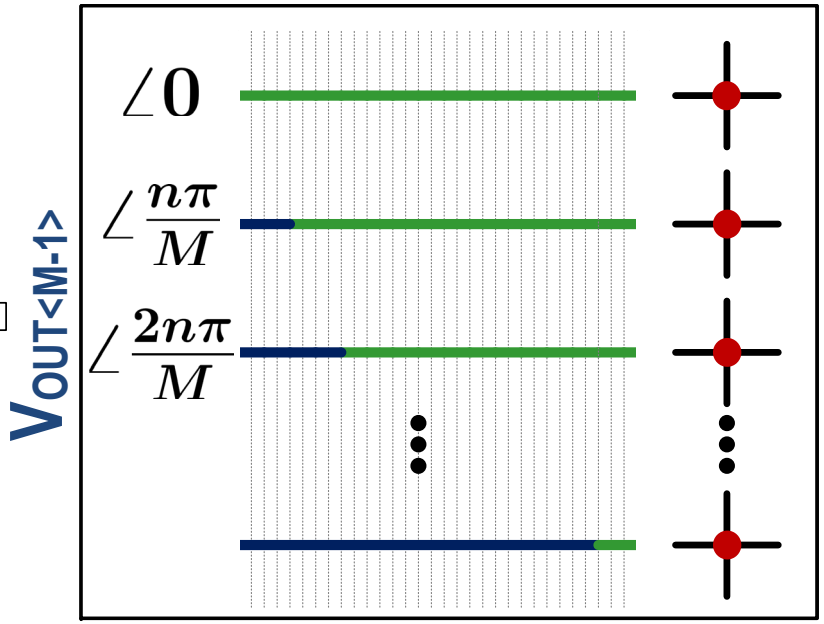
Technique 1: Harmonic-Rejection TIAs (3/5)



Inputs identical, but shifted by π/M → Gain

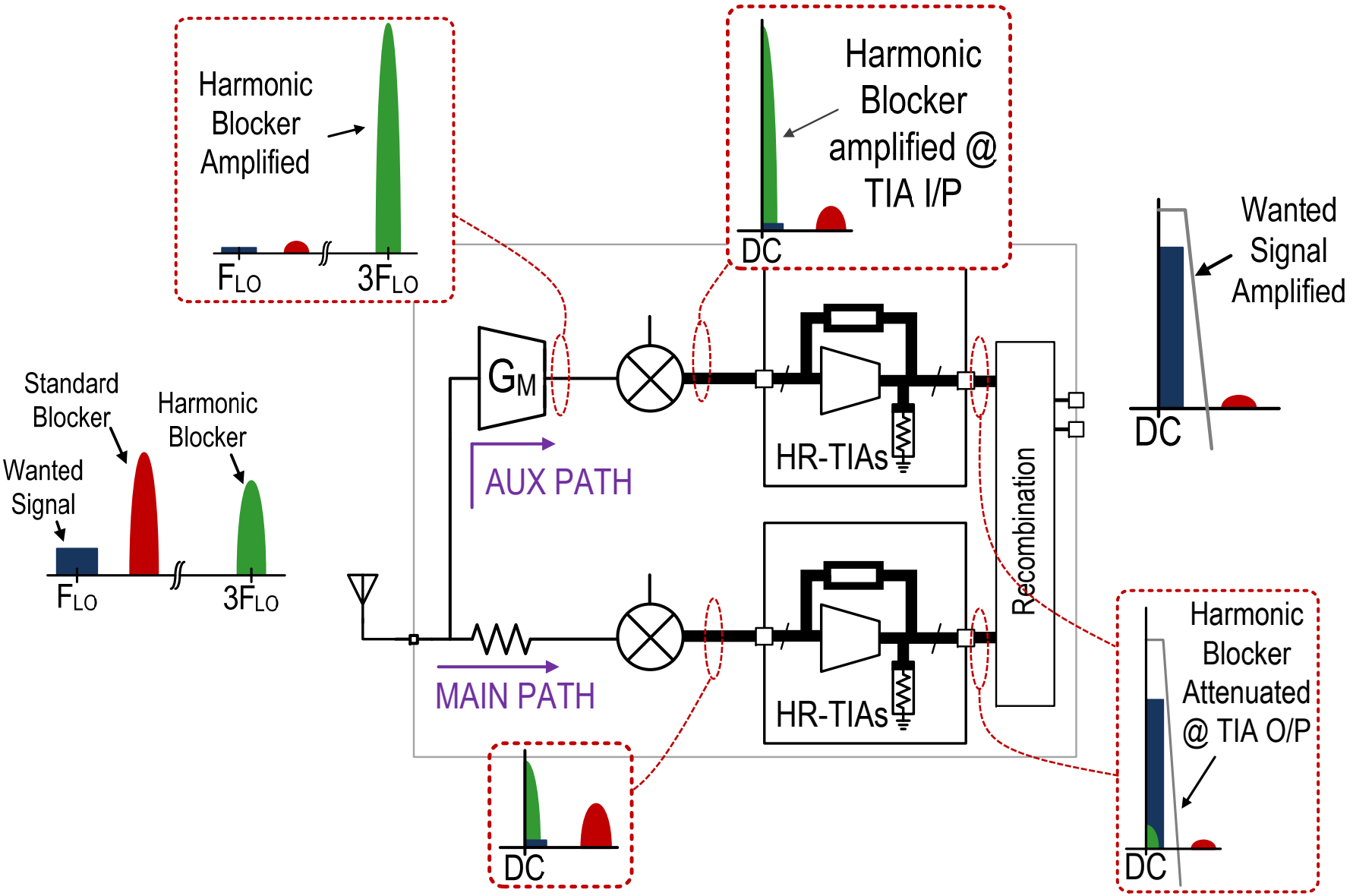
Technique 1: Harmonic-Rejection TIAs (4/5)



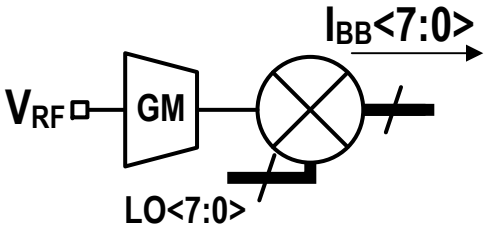


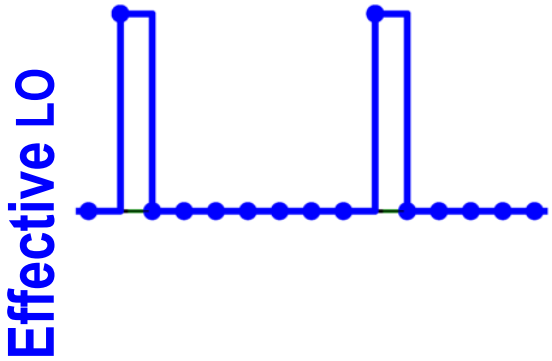
$$|V_{OUT}[X]| \approx \begin{cases} Z_F I_{RF}/M, & \text{if } f \approx F_{LO} \\ 0, & \text{otherwise} \end{cases}$$

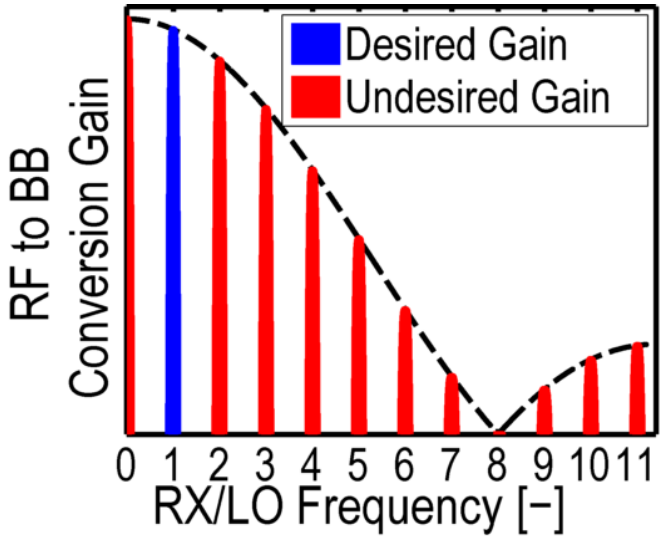
Technique 1: Harmonic-Rejection TIAs (5/5)

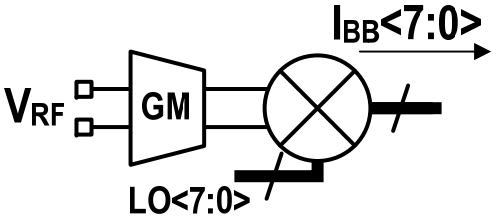


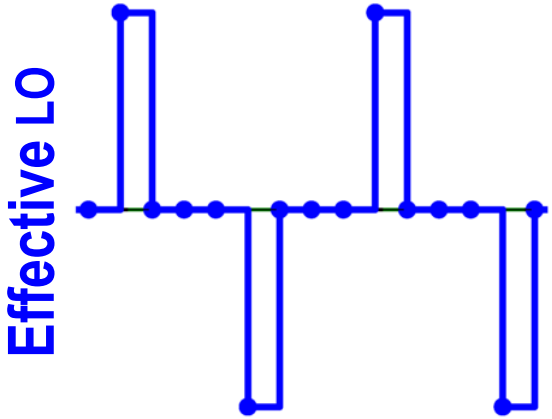
Technique 2: Multiple RF-GMs (1/2)

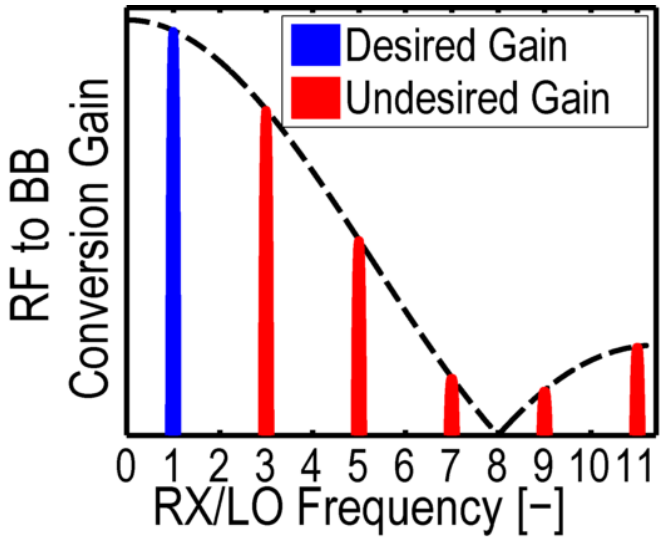




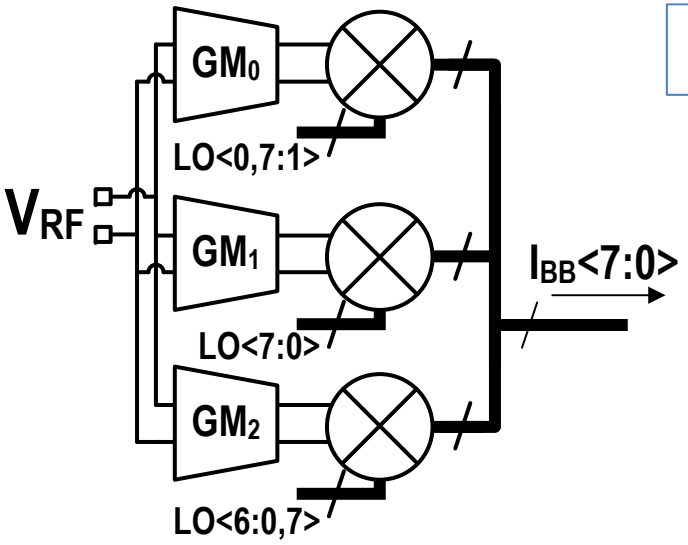








Technique 2: Multiple RF-GMs (2/2)



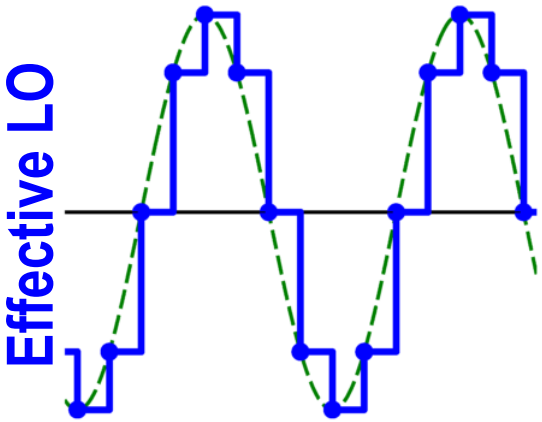
Ru et. al., ISSCC'09

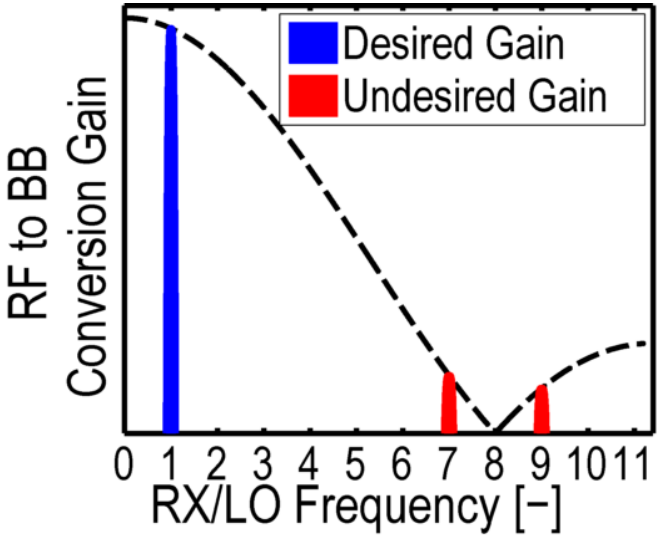
Emphasis …

→Improved Small-Signal HR

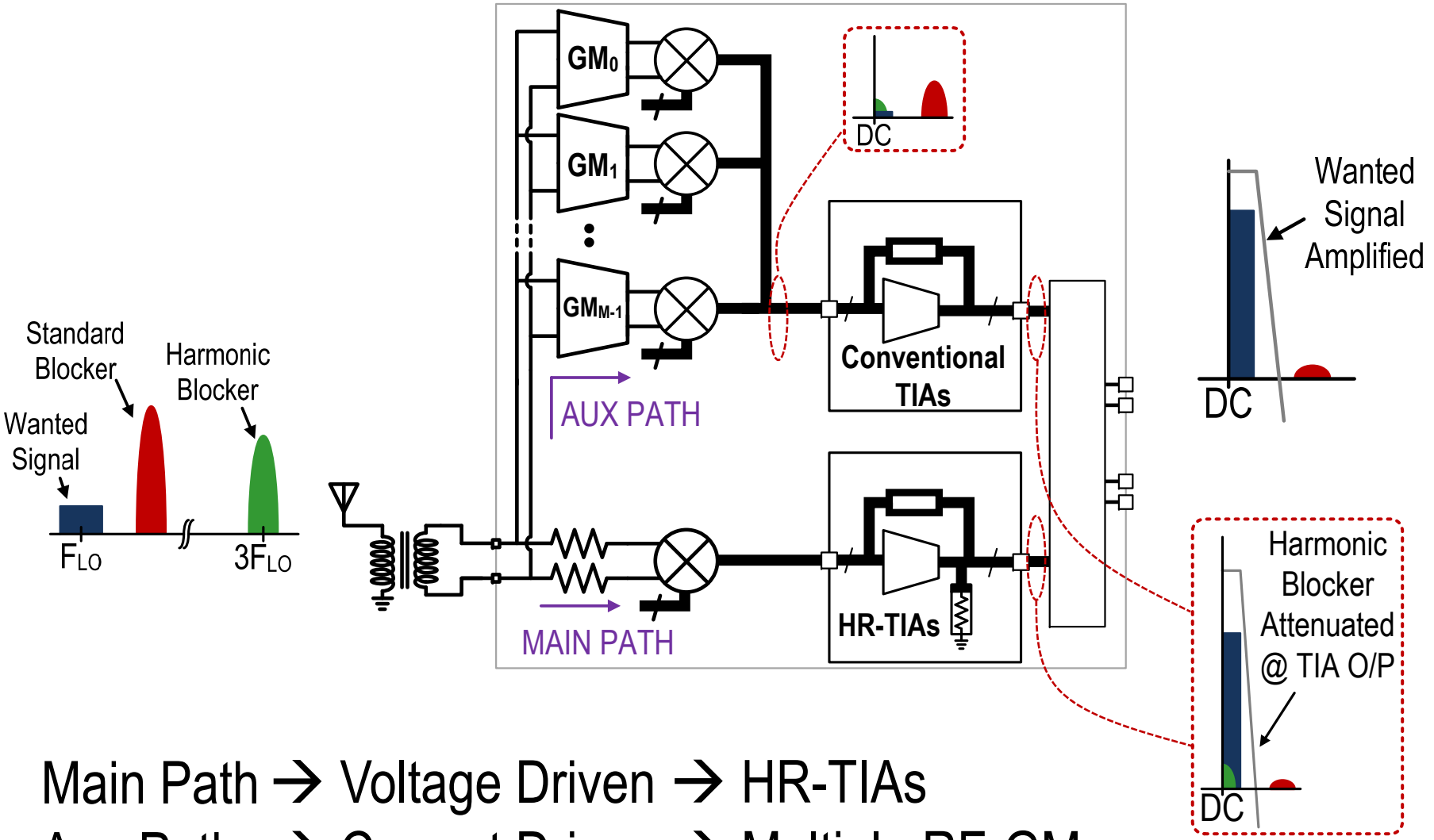
Also …

→ Enhances Large-Signal, Harmonic-Blocker Tolerance





Enhanced Noise-Cancelling Architecture

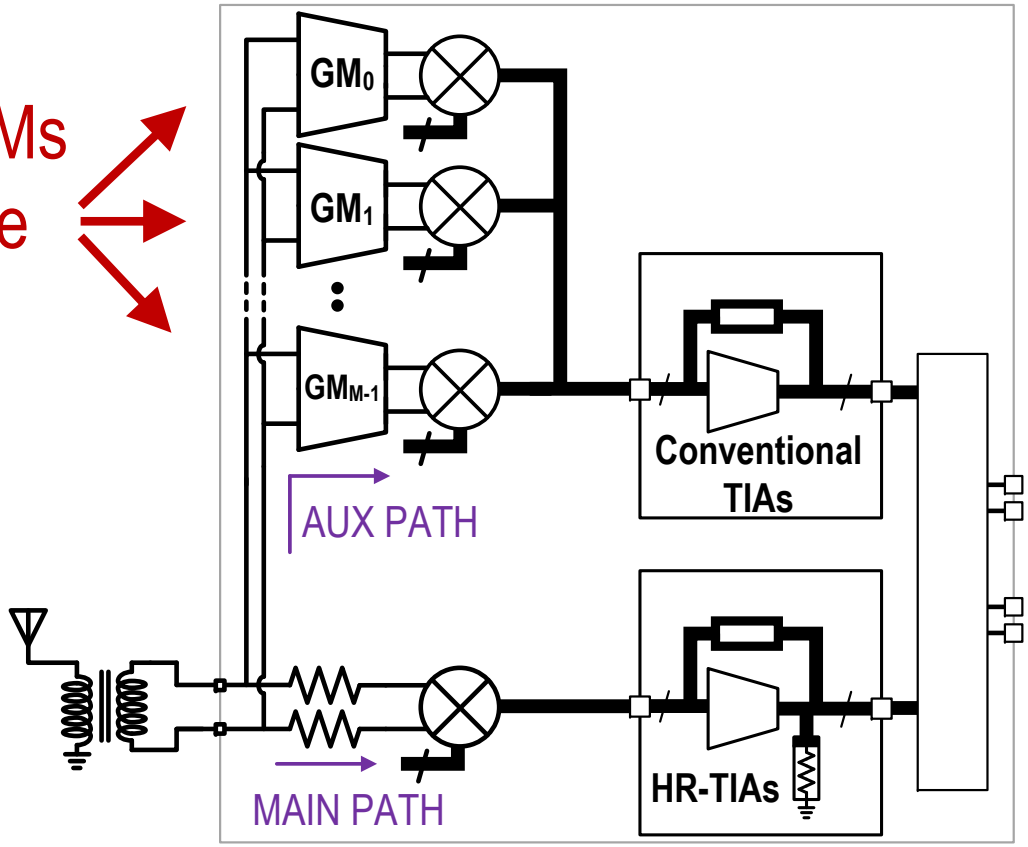


Main Path → Voltage Driven → HR-TIAs

Aux Path → Current Driven → Multiple RF-GMs

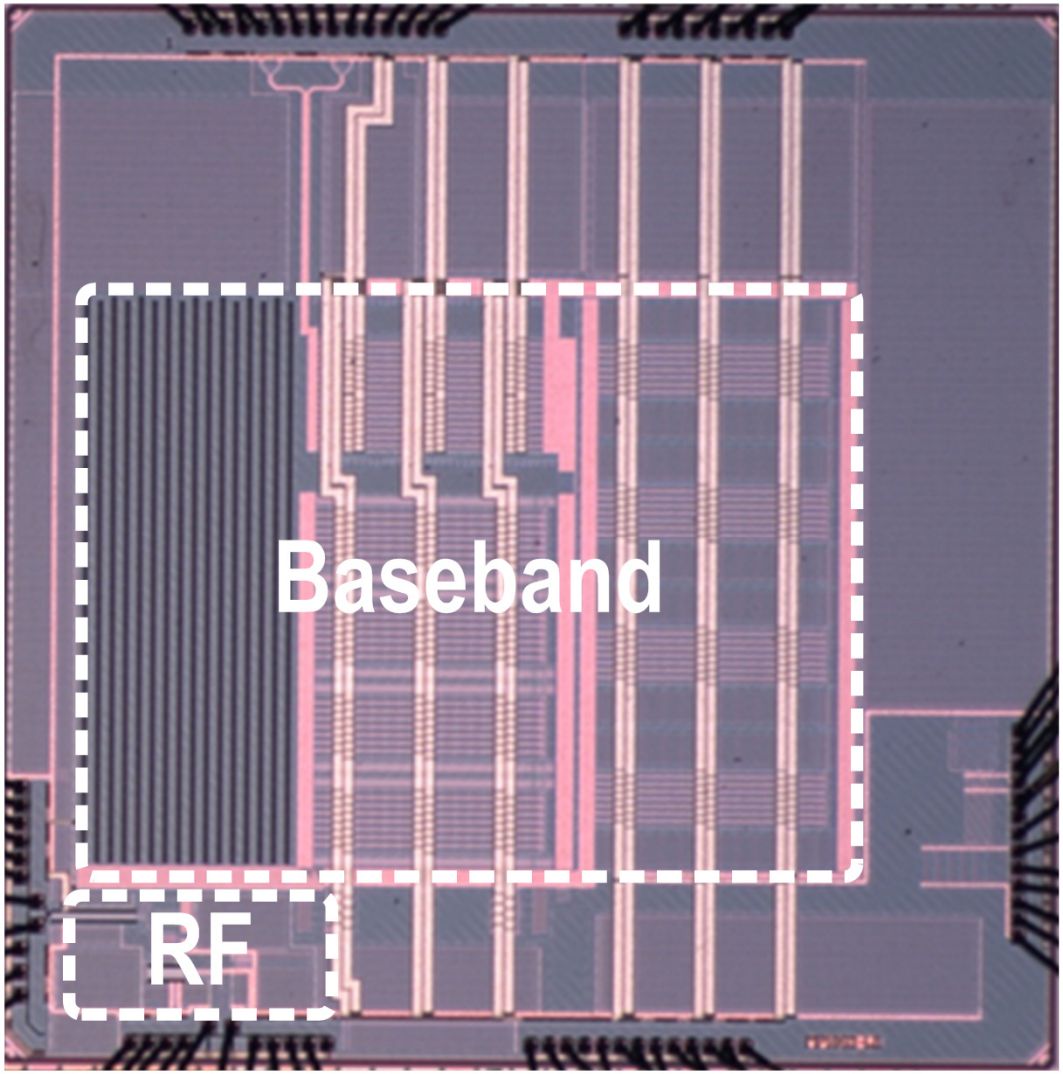
Noise Figure (Enhanced Architecture)

Multiple RF-GMs are only noise contributors



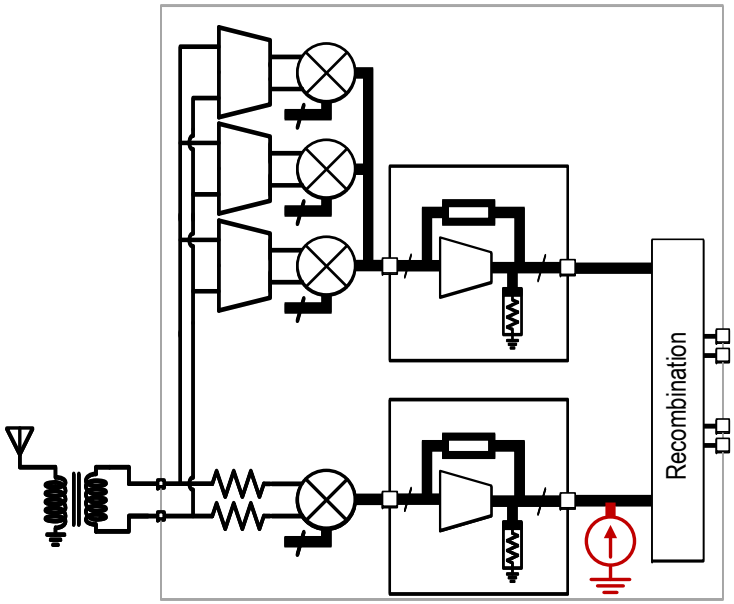
$$F \approx 1 + \frac{3}{2}\left(\frac{\overline{vn^2_{GM_0}} + \overline{vn^2_{GM_1}} \cdots}{4kT50}\right)$$

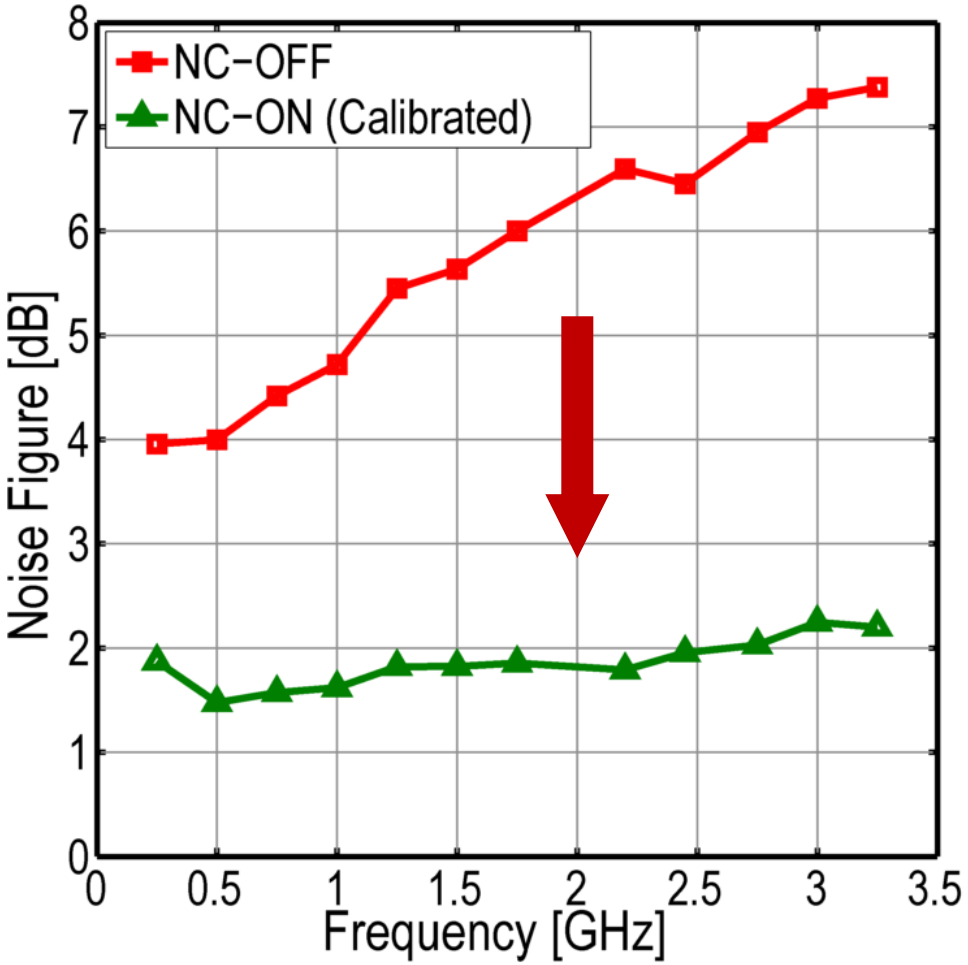
Die Micrograph



28nm, Inductor-less, 5mm^2 Active Area

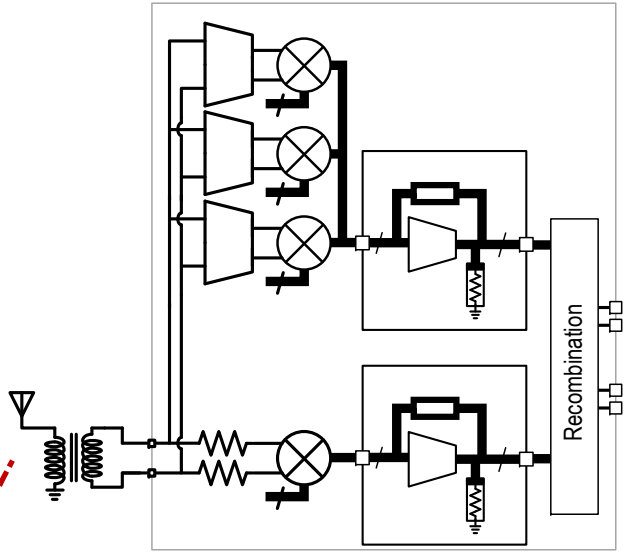
Measured Noise Figure

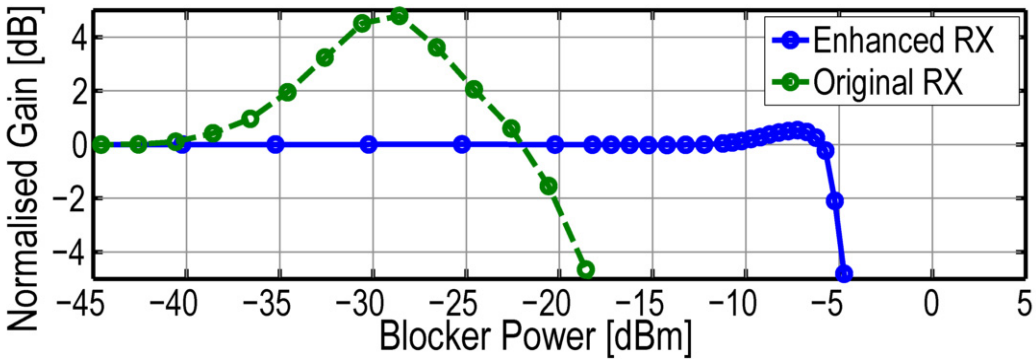


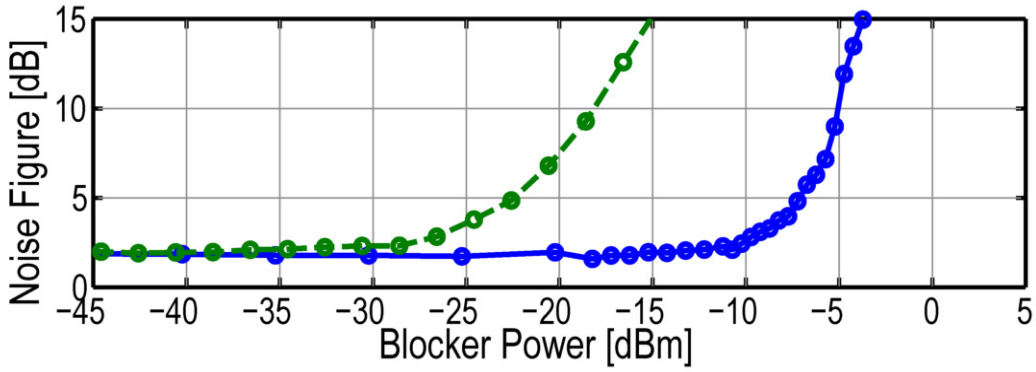


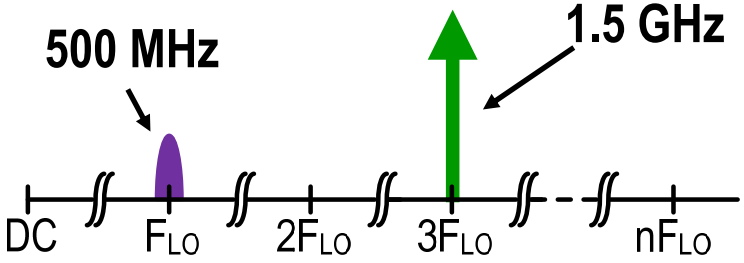
NF Calibration Scheme → Murphy et. al., CICC 2013

Measured Harmonic-Blocker Noise Figure



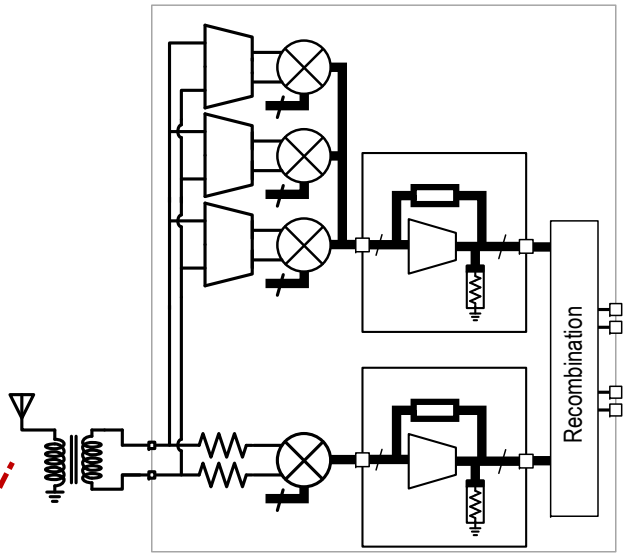


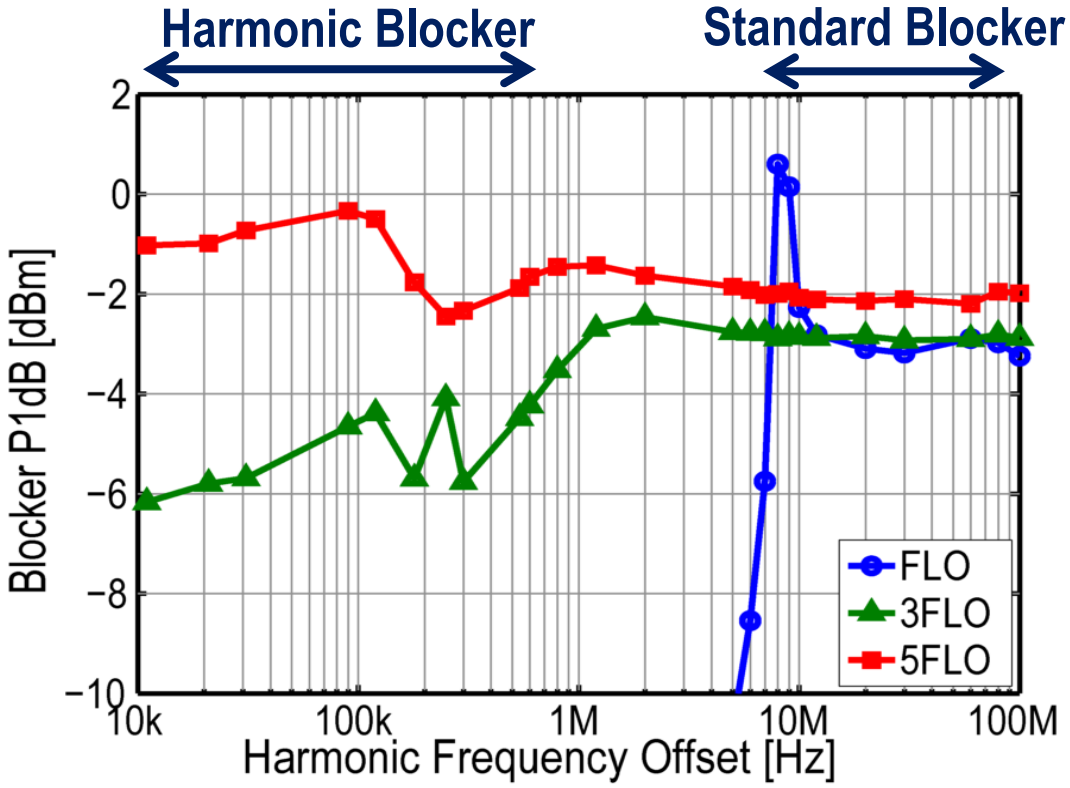


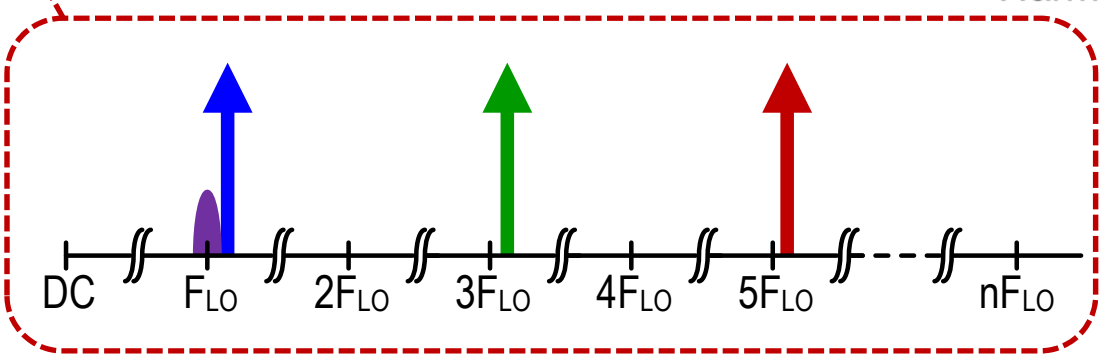


$3F_{LO}$ Harmonic Blocker:
P1dB = -6dBm
NF = 9dB @ -5dBm

Measured Harmonic-Blocker P1dB







Harmonic Blocker Test:

F_{LO} = 500MHz

IF Bandwidth = 200kHz

Comparison to other Low-Noise, Wideband RXs

	ISSCC'10 (Andrews et. al.)	VLSI'13 (Borremans et. al.)	ISSCC'12 (Murphy et. al.)	This Work	
Topology Description	Mixer-First	Resistive Feedback	FTNC-RX	Modified FTNC-RX	
CMOS Technology	65nm	28nm	40nm	28nm	
RF Input	Single-Ended	Differential	Single-Ended	**Differential**	**Single-Ended**
RX Frequency [MHz]	100-2400	400-3000	80-2700	100-3300	600-3000
NF @ 2GHz [dB]	7	2.3-2.9*§	1.9	**1.7***	**1.8 (low NF mode) 3 (HR mode)**
OB-P1dB [dBm]	4	N/A	-2	-2.5	-6
0dBm OB-Blocker NF [dB]	N/A	15	4.1	**5**	**9 (low NF mode) 13 (HR mode)**
Harmonic Blocker P1dB [dBm]	N/A	N/A	N/A	-6.5 ($3F_{LO}$) -3 ($5F_{LO}$)	-10 ($2F_{LO}$) -8 ($3F_{LO}$)
Harmonic Blocker NF [dB]	N/A	N/A	N/A	**9@-5dBm ($3F_{LO}$)**	**7@-7.5dBm ($2F_{LO}$) 9@-7.5dBm ($3F_{LO}$)**
Supply Voltage [V]	1.2/2.5	0.9	1.3	1.0	1.0
OB-IIP3 [dBm]	+25	+3	+13.5	+11.5	+10
OB-IIP2 [dBm]	+58	85¥	+54	+55	+49.5
Harmonic Rejection [dB] $3F_{LO}/5F_{LO}$	35.4/42.6	70/55¥	42/45	**≈60/60**	**≈52/54 ($3F_{LO}/5F_{LO}$) ≈60/60 ($2F_{LO}/4F_{LO}$)**
Total Power [mW]	37-70	40	35.1-78	36.8-62.4	38.8-70
Active Area [mm^2]	2	0.6	1.2	5.2	5.0

*Balun loss not included §In high linearity mode. ¥With calibration

Conclusions

- An improved noise-cancelling receiver is presented
  - Enhanced resilience to harmonic blockers
  - Maintains sub-2dB noise figure
- Fabricated 2 prototypes that validated architecture
  - Fully differential design
  - Reconfigurable design with single RF input
- Validated a NF calibration method

A Fully Integrated TV Tuner Front-End with 3.1dB NF, >+31dBm OIP3, >83dB HRR3/5 and >68dB HRR7

In-Young Lee[1], Sang-Sung Lee[1], Donggu Im[2], Seungjin Kim[1], Jeongki Choi[3], Sang-Gug Lee[1], Jinho Ko[3]

[1]KAIST, Daejeon, Korea

[2]University of Texas, Dallas, Richardson, TX

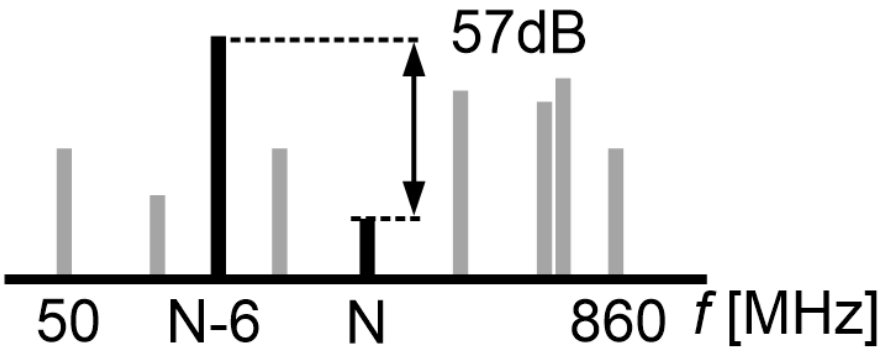
[3]PHYCHIPS, Daejeon, Korea

Outline

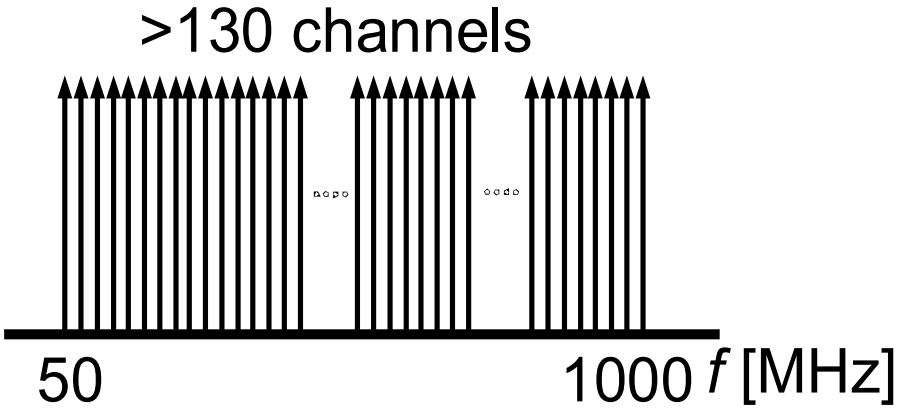
- TV tuner front-end design issue
- Proposed tuner front-end
  - Linear 4th-order RF low-pass filter
  - Gain- & linearity-boosting LNA
  - Robust harmonic rejection mixer
- Implementation
- Measurement
- Conclusion

General issues in TV tuner design

Terrestrial

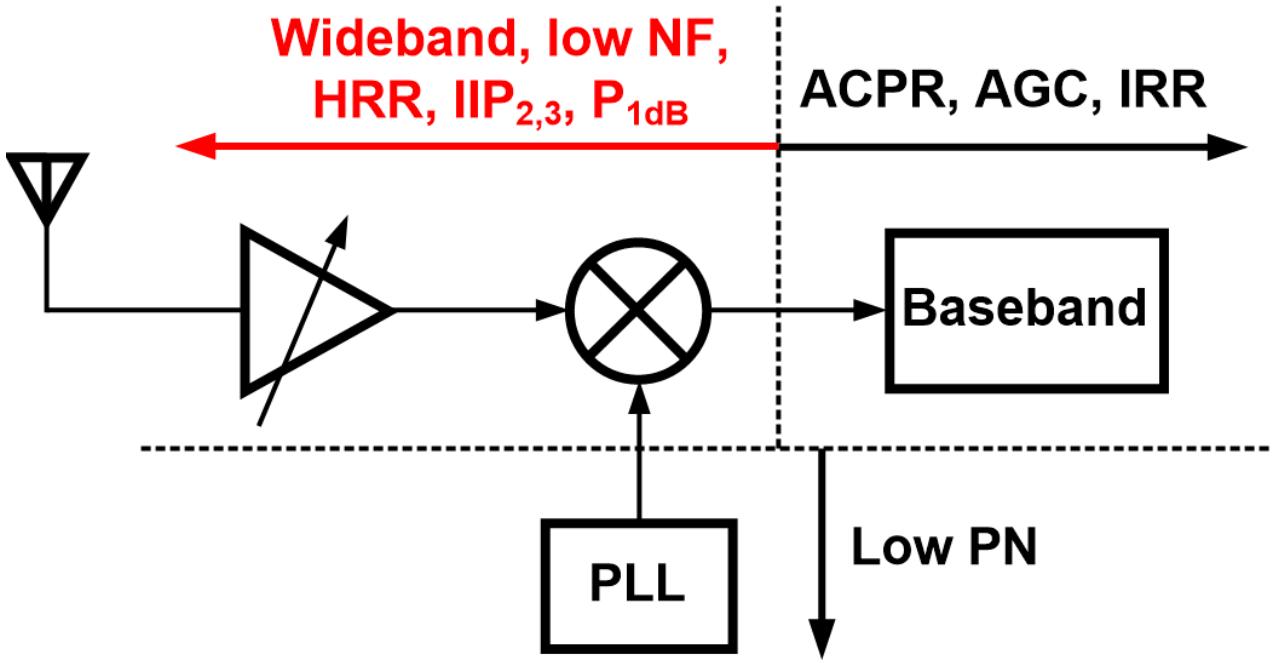


Cable



- Desensitization
  - Desensitization (P_{1dB})
- Harmonic rejection
- High linearity even with high-power inputs
  - IIP3, IIP2 [CTB, CSO]
- Image rejection
- Low phase noise
- Intelligent AGC

Front-end design issues



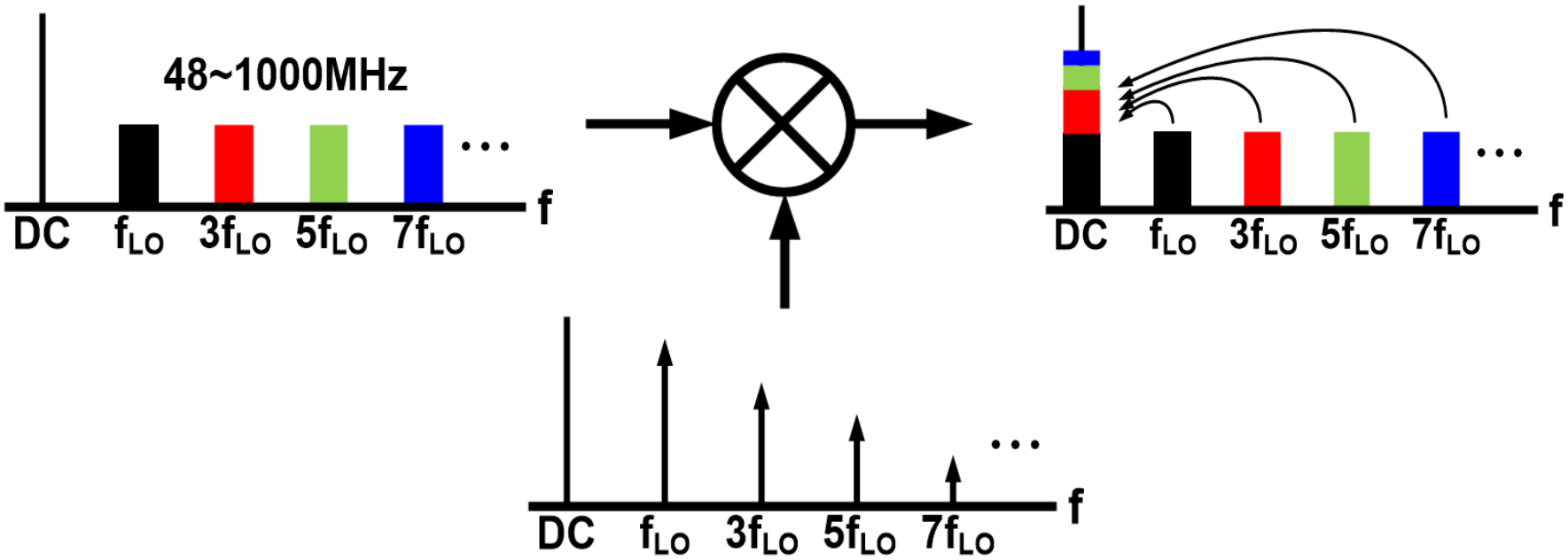
	Freq. [MHz]	NF [dB]	HRR [dB]	OIP3/OIP2 [dBm]	Pin [dBm]
RF front-end	48-1000	<6.45 (*<4dB)	>70	>25 / >55	-83 ~ -8

***for ATV (NTSC, PAL)**

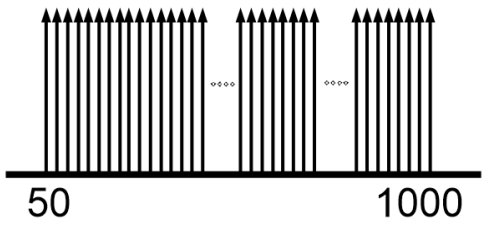
[JSSC'13 Greenberg, "A 40-MHz-to-1GHz Fully Integrated Multistandard Silicon Tuner in 80-nm CMOS"

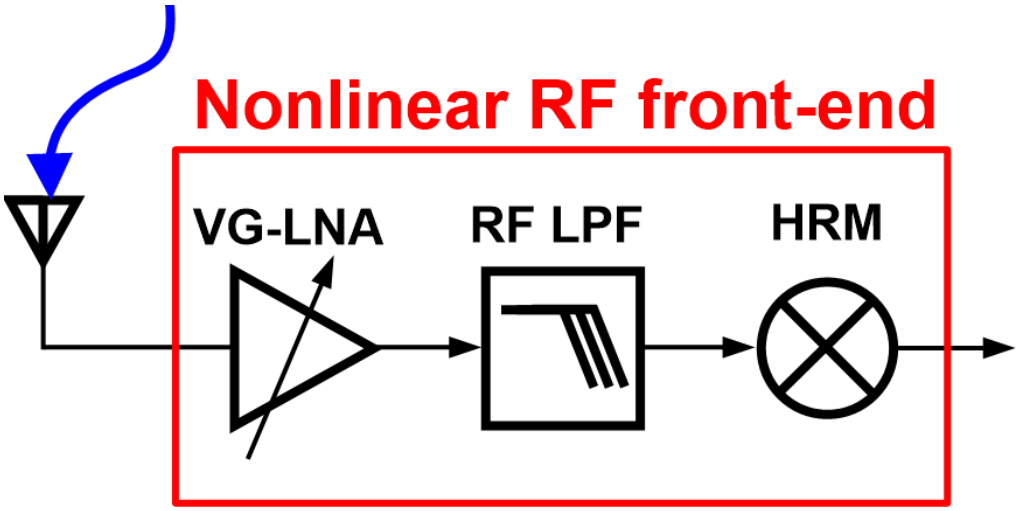
Harmonic mixing

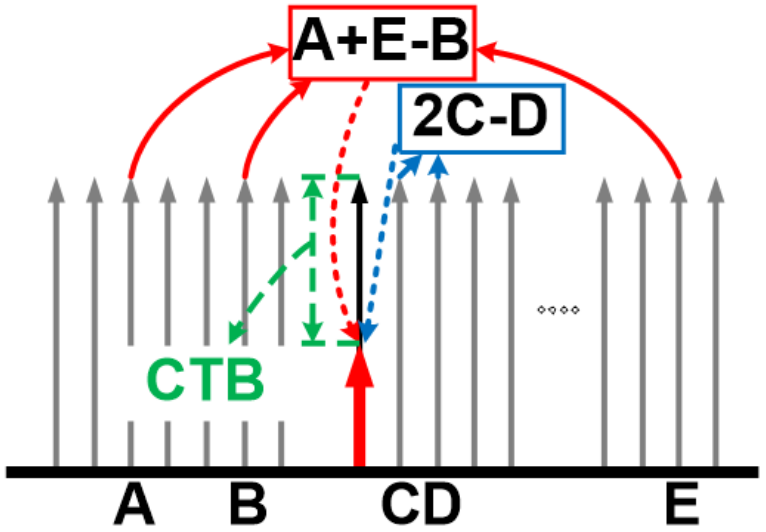
- ISSCC' 09 B. Nauta : > 60dB for 3rd and 5th HRR
- **7th and higher order HRR → RF Filter required!**

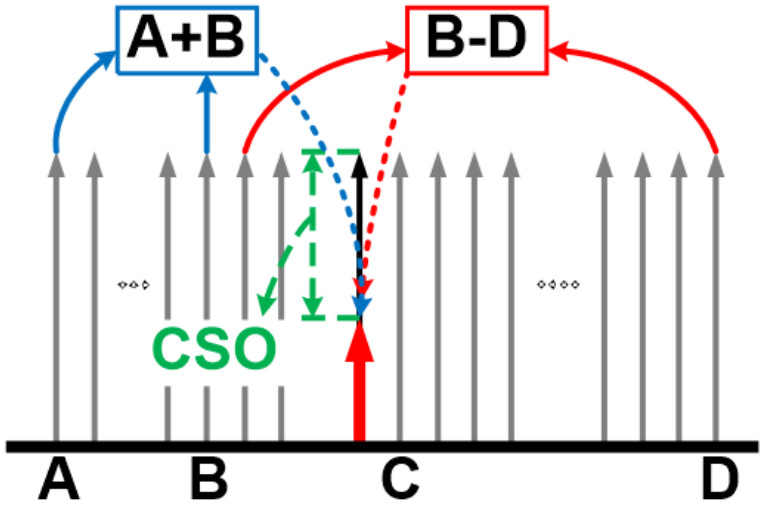


Intermodulation





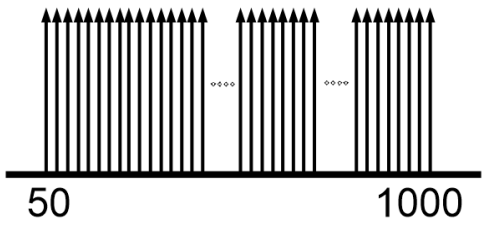


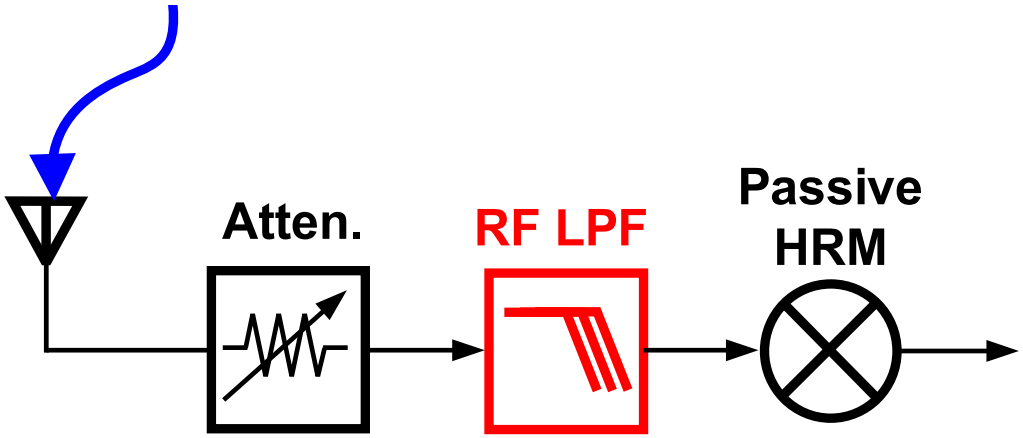


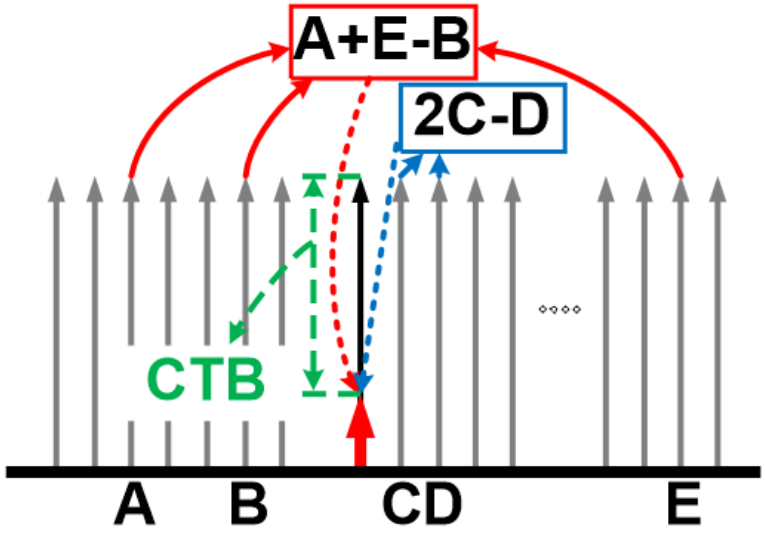
- >60dB CTB, CSO required

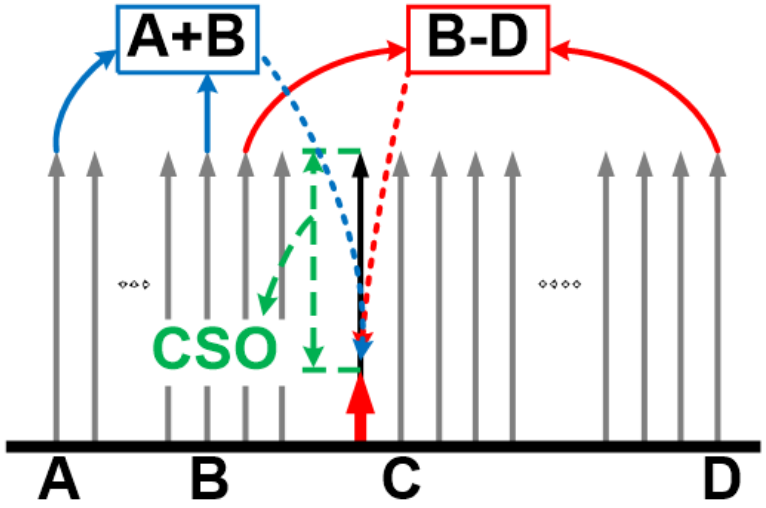
  → front-end OIP2/3: >55/>25dBm

Linearity bottleneck





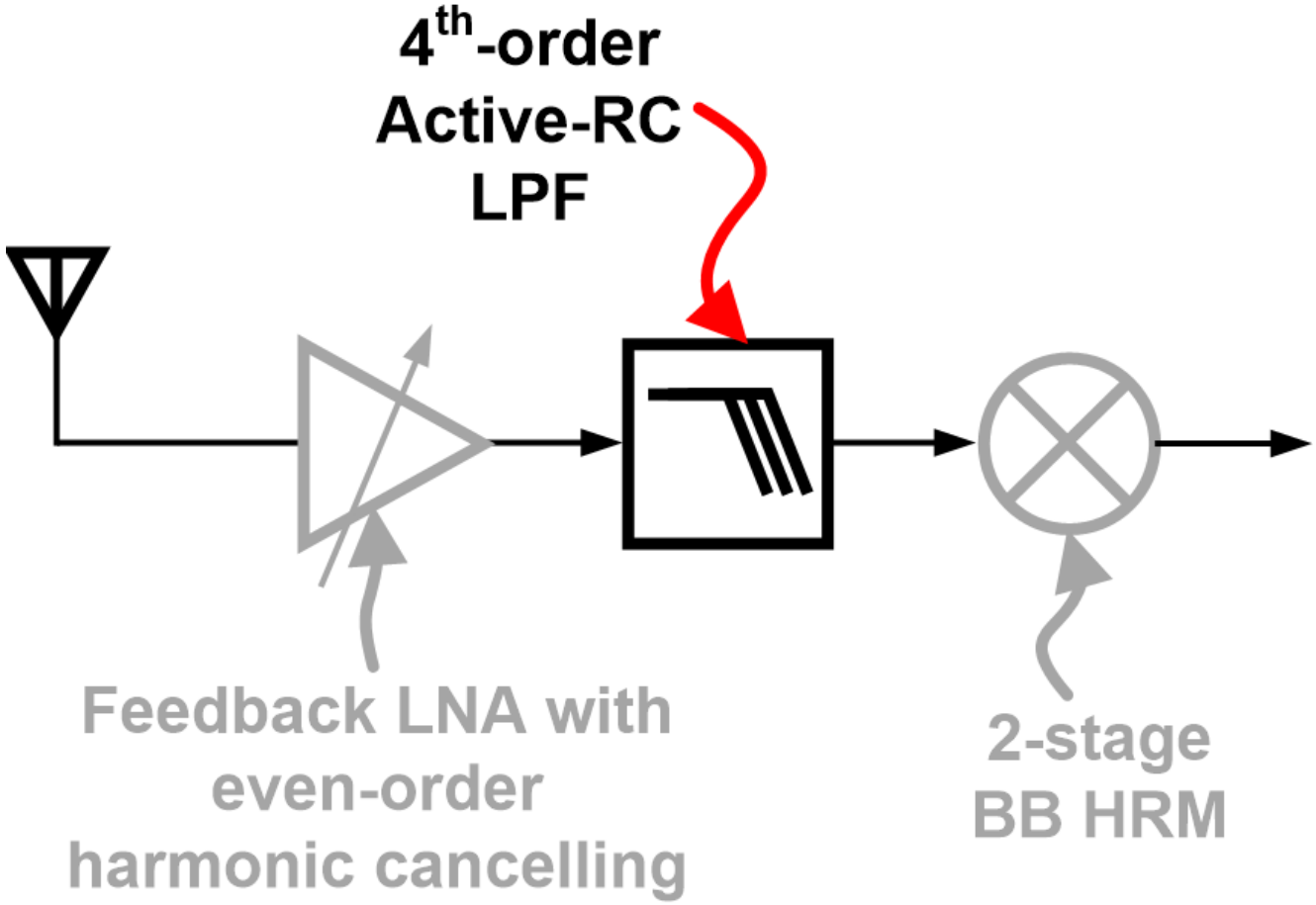




[ISSCC'12 Greenberg, TCAS-I'11 Kwon]

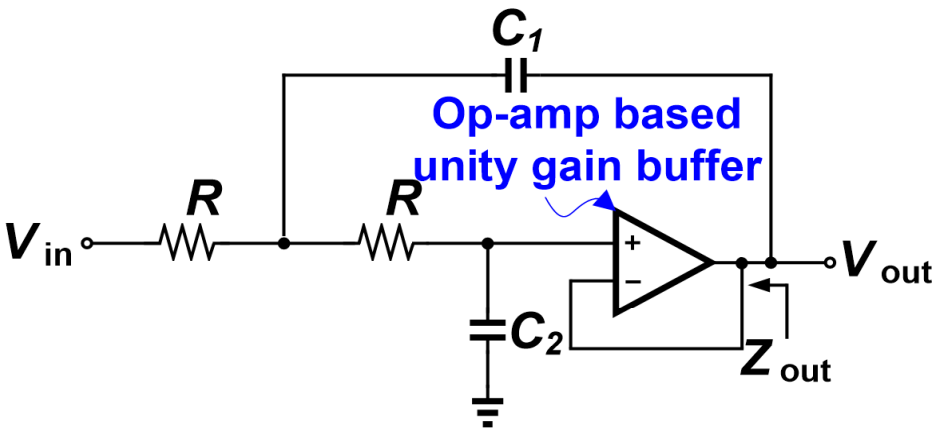
- NF: 15~16dB
- IIP3 (OIP3): 16~17dBm
  for 3rd Chebyshev, 4th Butterworth

Highly linear TV tuner front-end [RF LPF]

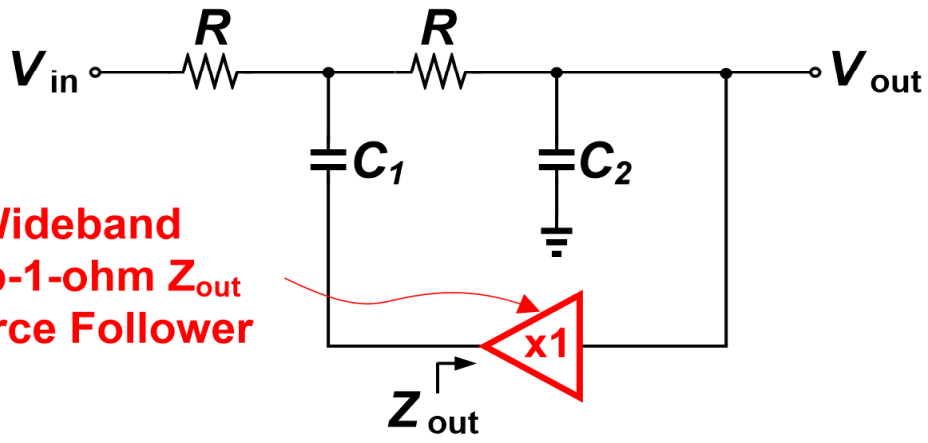


Filter topology

Sallen-Key filter topology

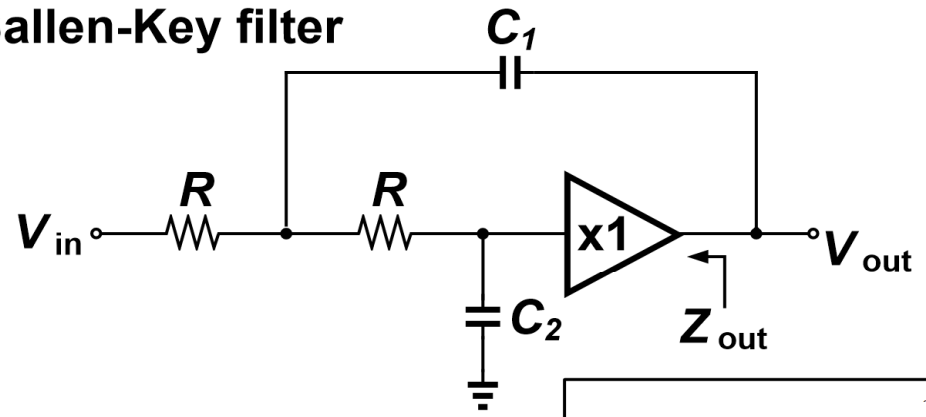


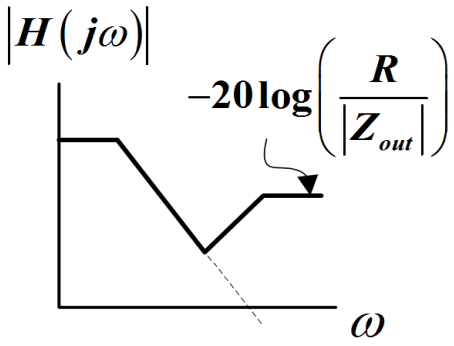
Proposed filter topology



Stop-band rejection limitation

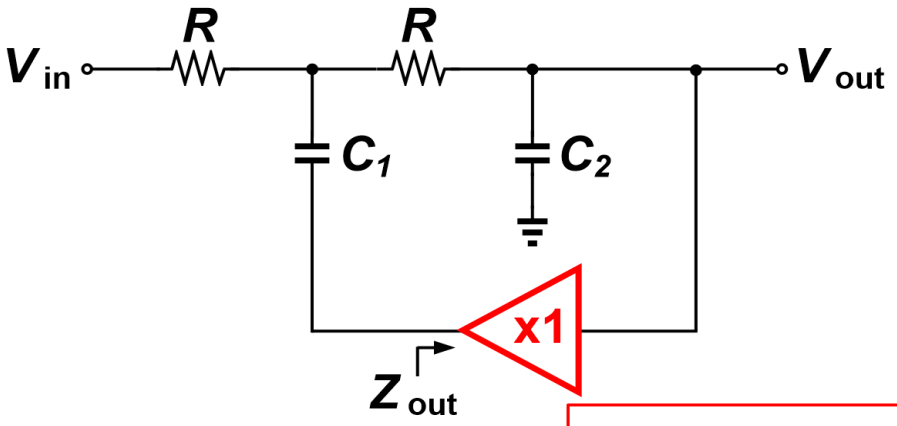
Sallen-Key filter

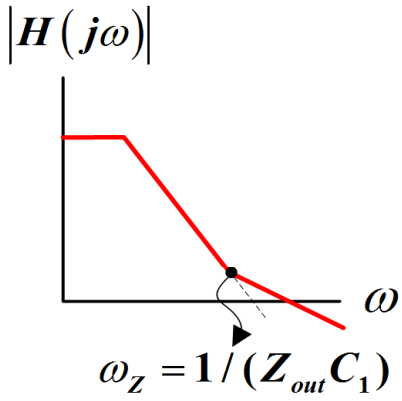




$$H(s)=\frac{1+sC_1Z_{out}+s^2C_1C_2RZ_{out}}{1+s\left(2C_2R+C_1Z_{out}\right)+s^2\left(C_1C_2R^2+2C_1C_2RZ_{out}\right)}$$

Proposed filter





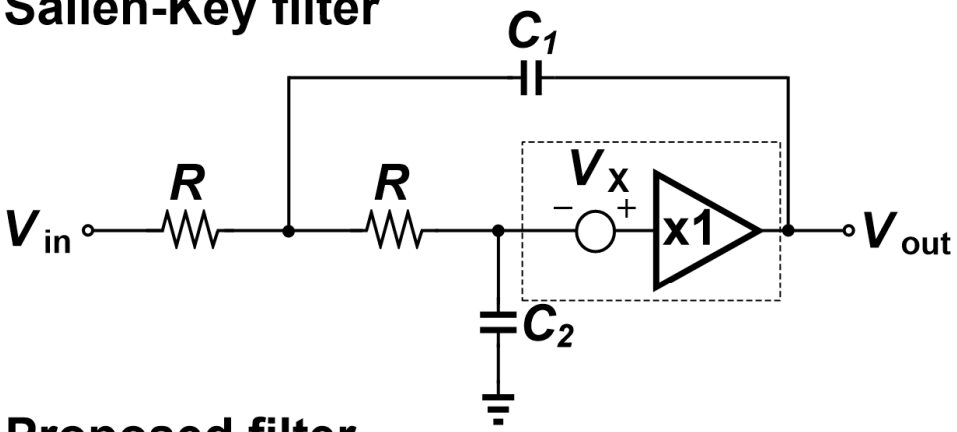
Remove 1 zero

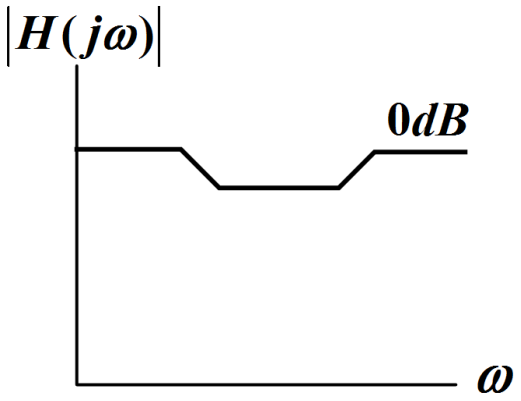
$$H(s)=\frac{1+sC_1Z_{out}}{1+s\left(2C_2R+C_1Z_{out}\right)+s^2\left(C_1C_2R^2+2C_1C_2RZ_{out}\right)}$$

Architectural benefits

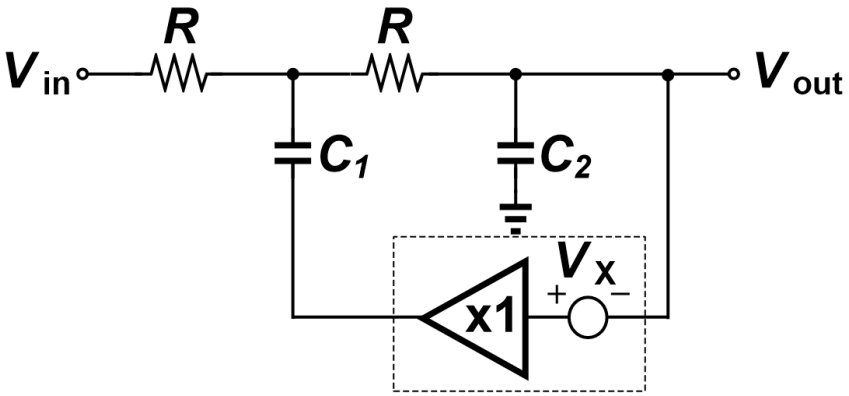
- Filter out 1/f noise, IMD components, DC offset vtg
- Operate like a passive filter in band

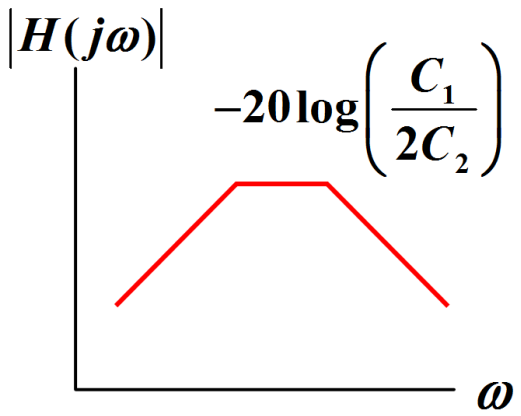
Sallen-Key filter





Proposed filter

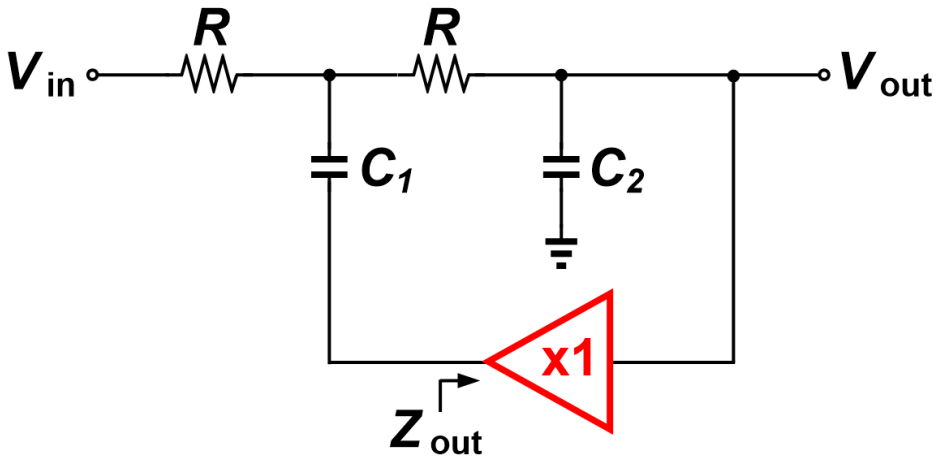




Z_{out} vs Q-factor / NF

- **Low Z_{out} wideband unity-gain buffer REQUIRED!**

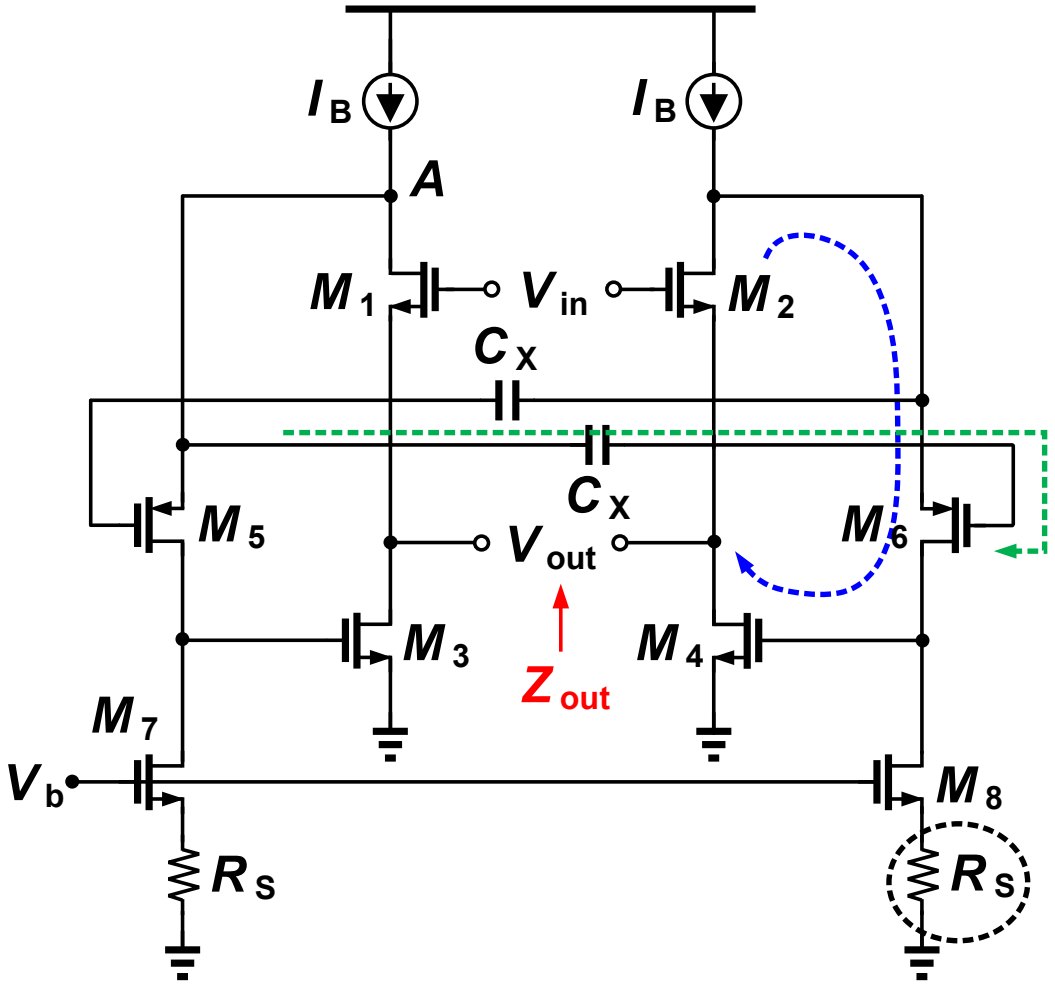
Lower Z_{out} → Higher Q → Steeper roll-off @ f_{high}
→ Lower R → Better filter NF
→ Push poles & zeros further → Wideband



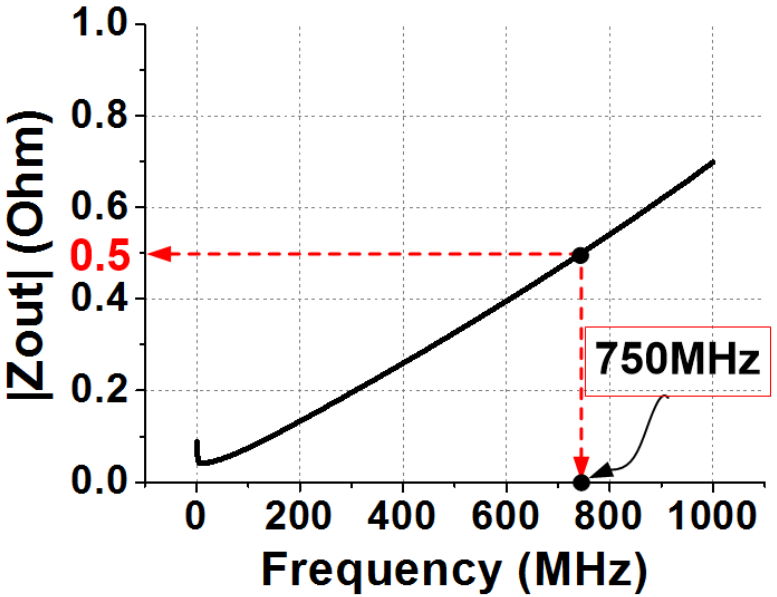
$$\frac{Z_{out}}{R} < \frac{1}{2\left(4Q^2-1\right)}$$

$$H(s) = \frac{1+sC_1Z_{out}}{1+s\left(2C_2R+C_1Z_{out}\right)+s^2\left(C_1C_2R^2+2C_1C_2RZ_{out}\right)}$$

Sub-1-Ohm Z_{out} source follower

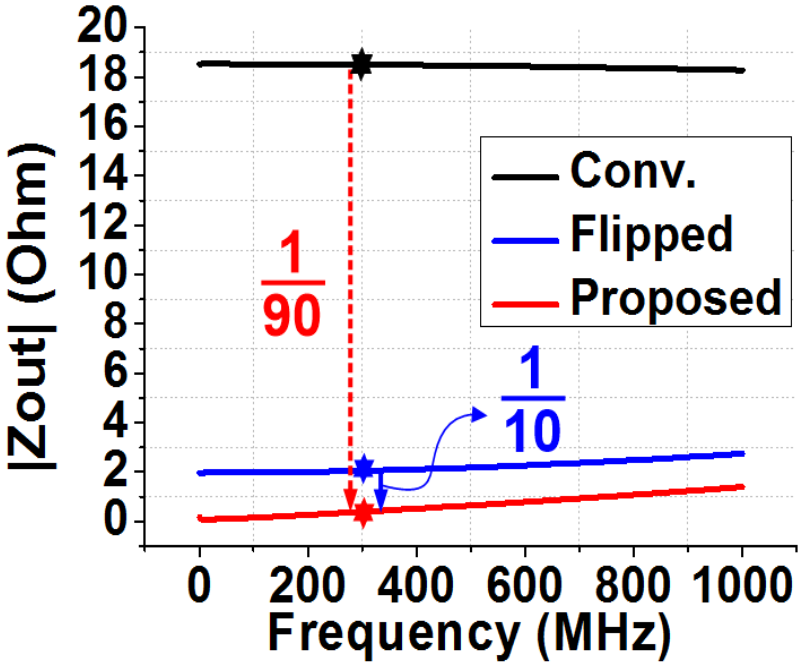


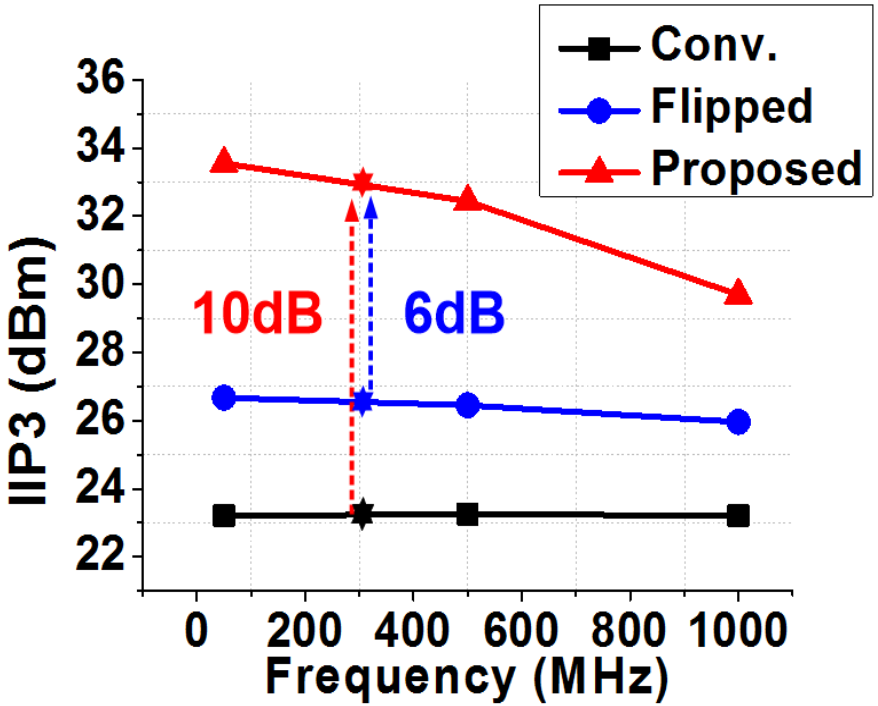
$$Z_{out\_proposed} \simeq \frac{1}{g_{m2}g_{m4}g_{m6}r_{o2}r_{o6}}$$



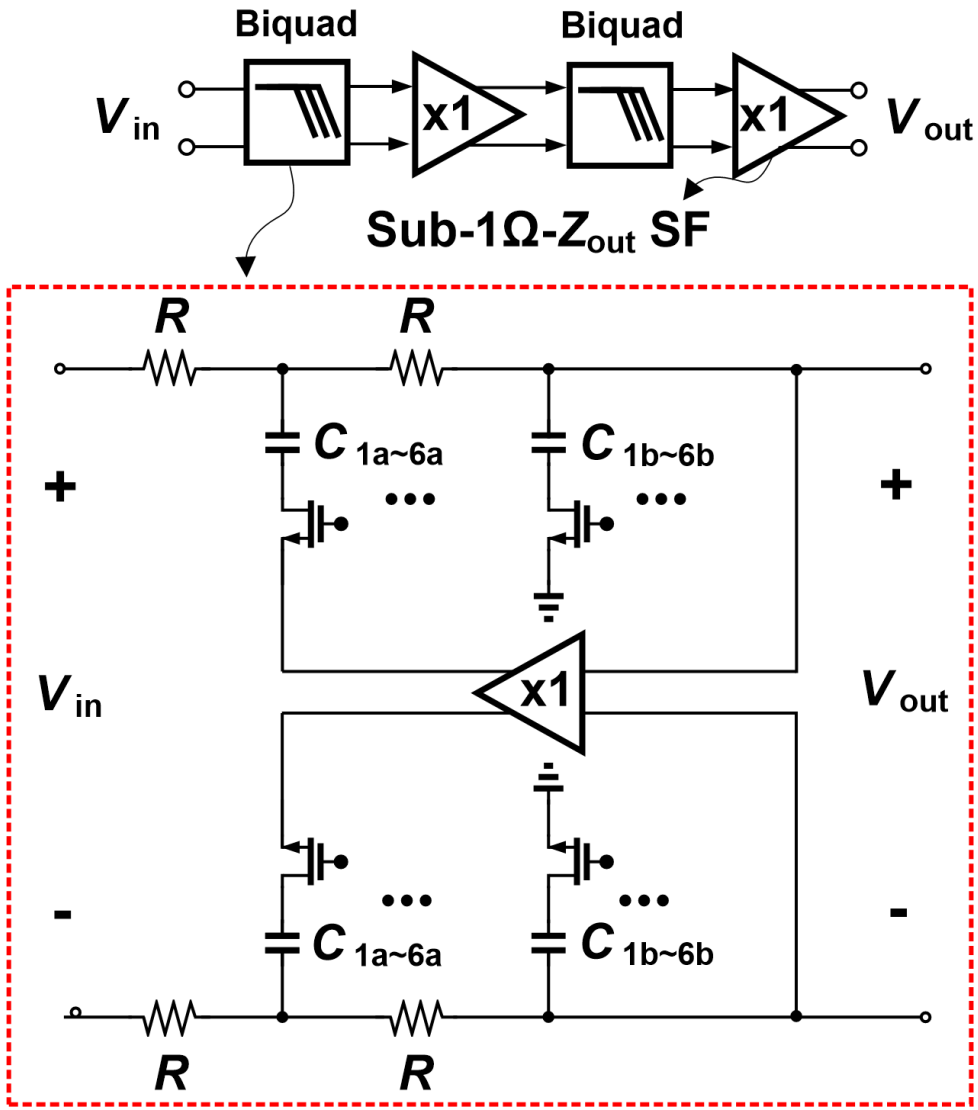
- **CG(M_6) Feedback, Cross-coupling (C_x), Z_{out_M8} boost (R_S)**

Z_{out} / IIP3 comparison





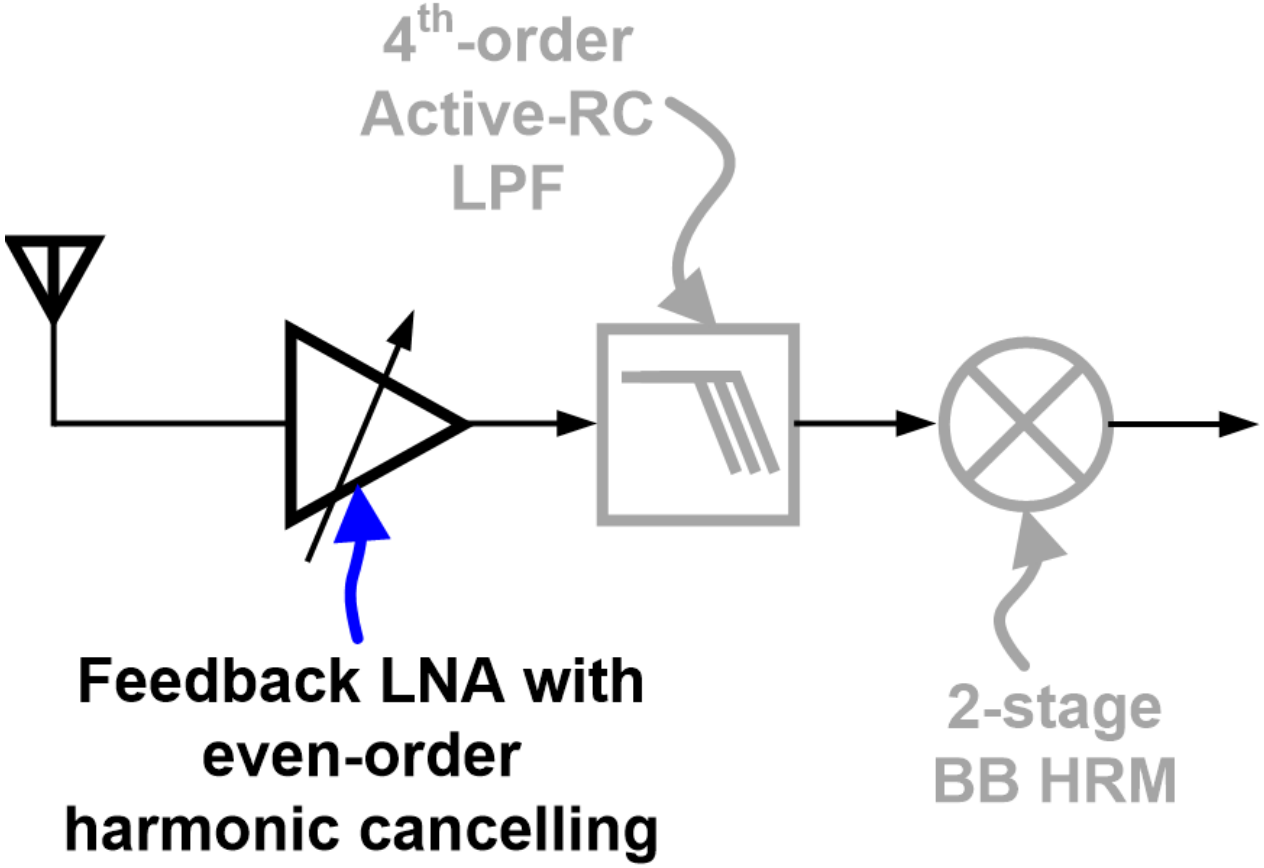
4th-order Active-RC LPF



Post-layout simulation

Type	Active-RC
Order	4
BW	40 ~ 660MHz
NF	<15dB
IIP_3	>25dBm
P_{1dB}	+10dBm
Power	32mA / 1.5V

Highly linear TV tuner front-end [WB LNA]

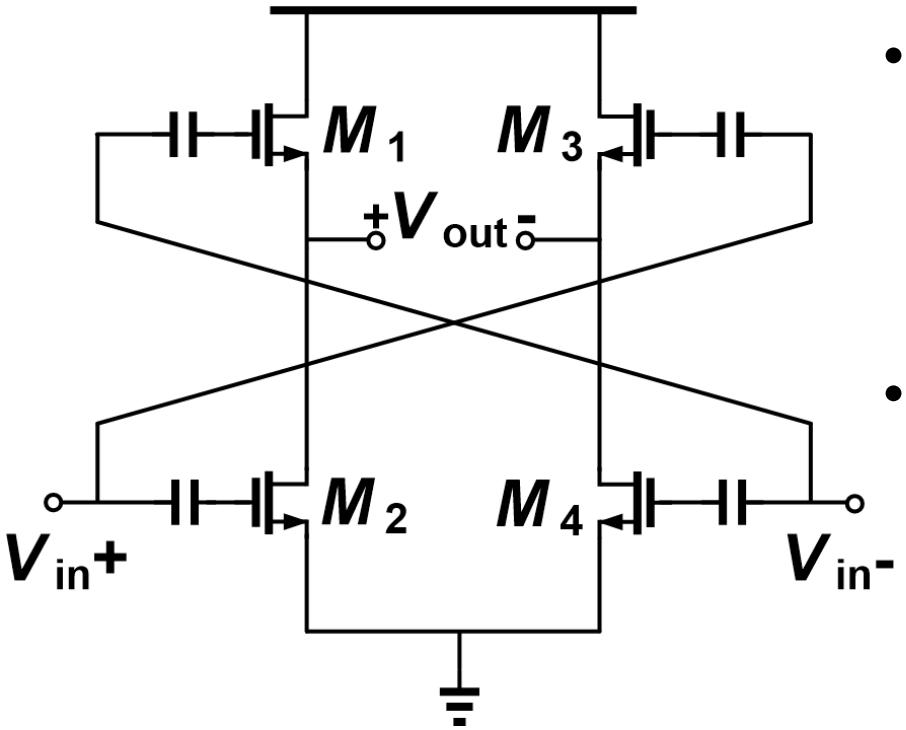


Linearization Techniques

Linearization Methods	gm				Cons.
	2^{nd}-order	3^{rd}-order	2^{nd}-order Interaction	Higher order	
Feedback	O	O		O	
Harmonic termination		O	O		IND /Narrow BW
Optimal biasing		O			PVT vari., Small P_{in}
Derivative superposition	O	O			PVT vari., Small P_{in}
IM2 injection		O	O		Narrow band only
Noise/distortion cancellation	O	O			Aux. path noise/dist.
Post-distortion	O	O			

Differential Hybrid Voltage Follower

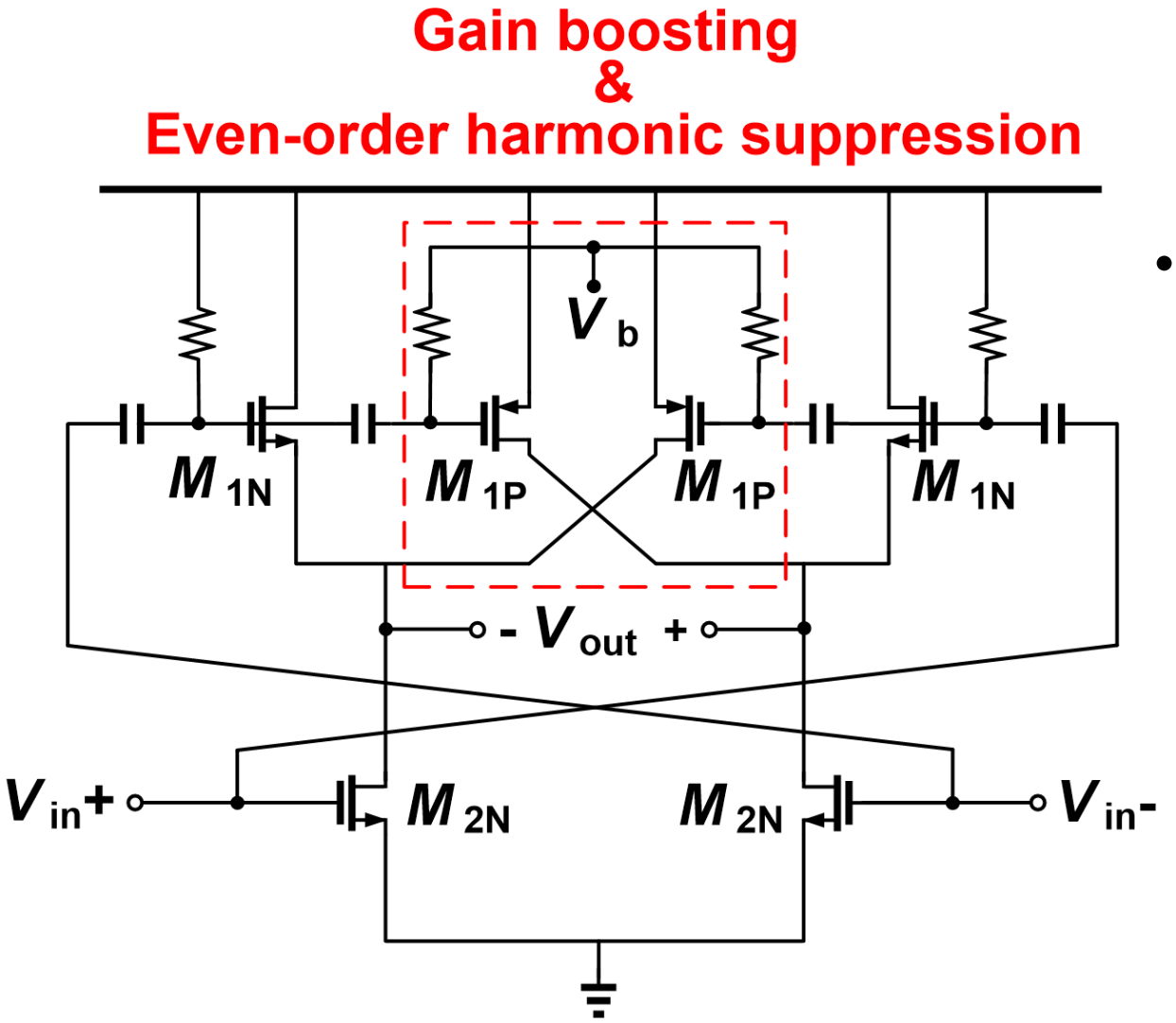
[T-MTT'09 Im (KAIST)]



- Gain : function of g_{m2}/g_{m1}
  - High linearity
  - M_2 distortion suppressed by M_1
- CS-CD cross-stacked
  → boost gain & lower noise

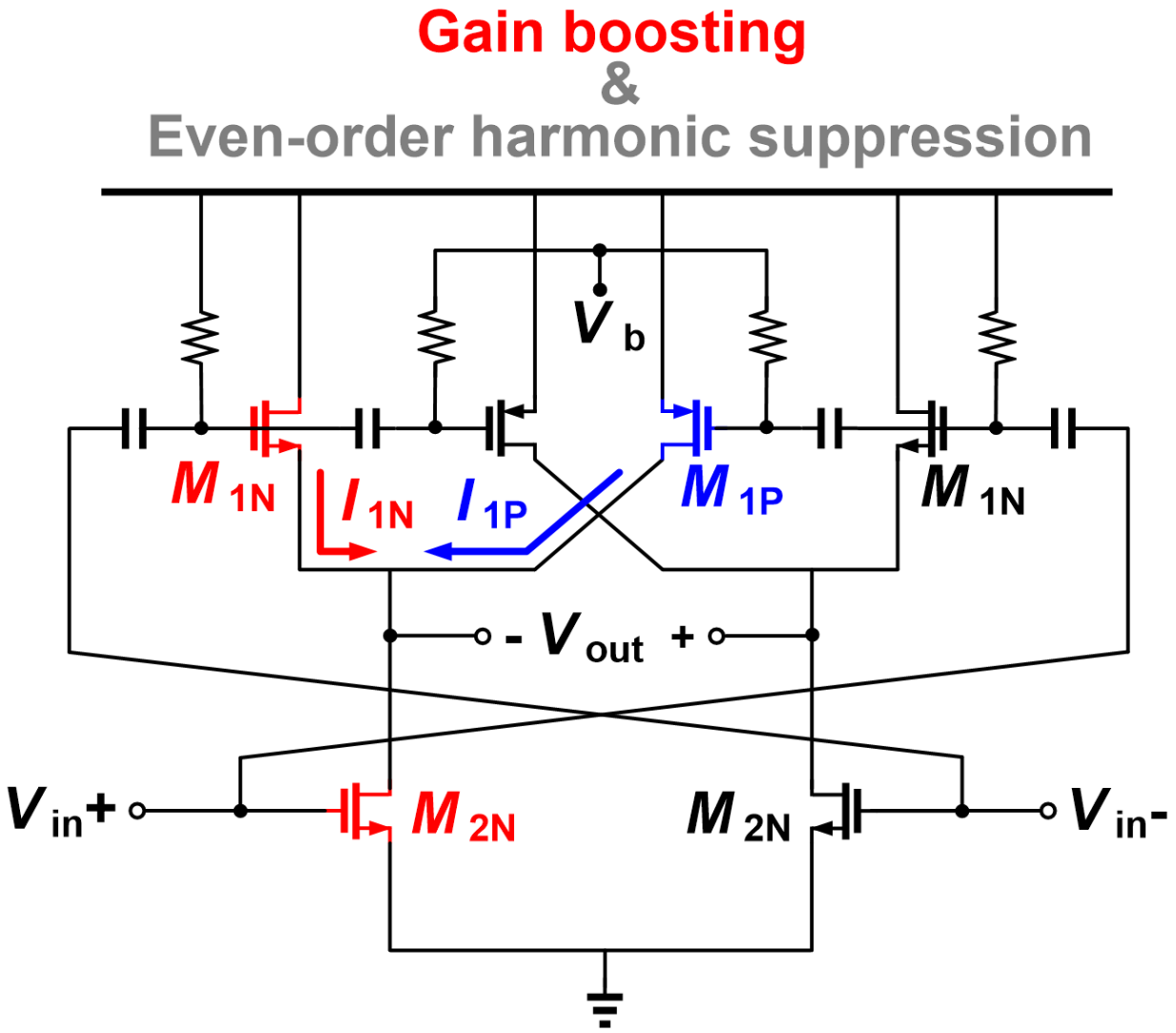
Gain is limited by voltage headroom!

Gain boost & Even-order dist. suppression



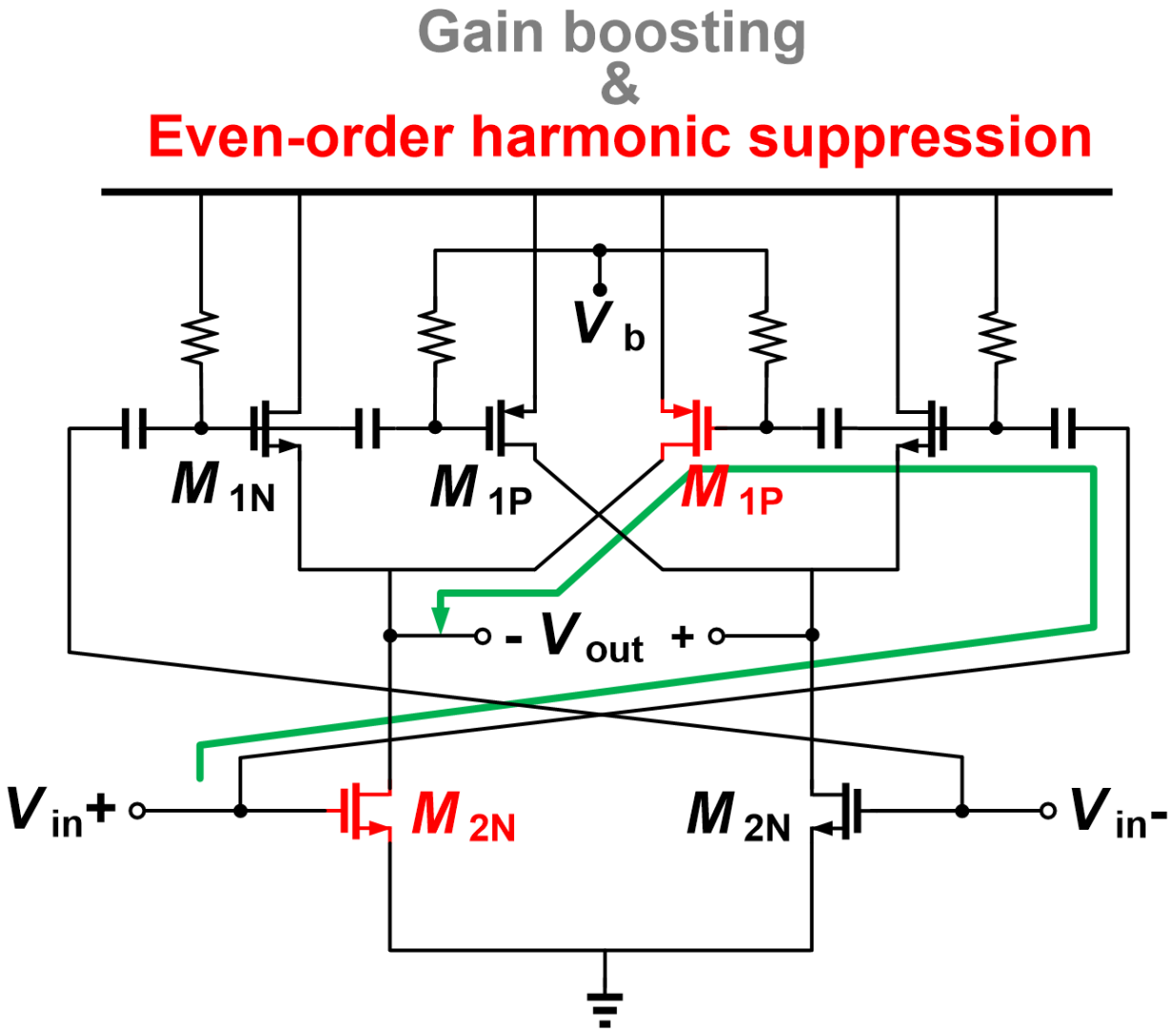
- Cross-coupled M_{1P} provides
  - Gain boosting
  - Even-order distortion suppression

Gain boosting



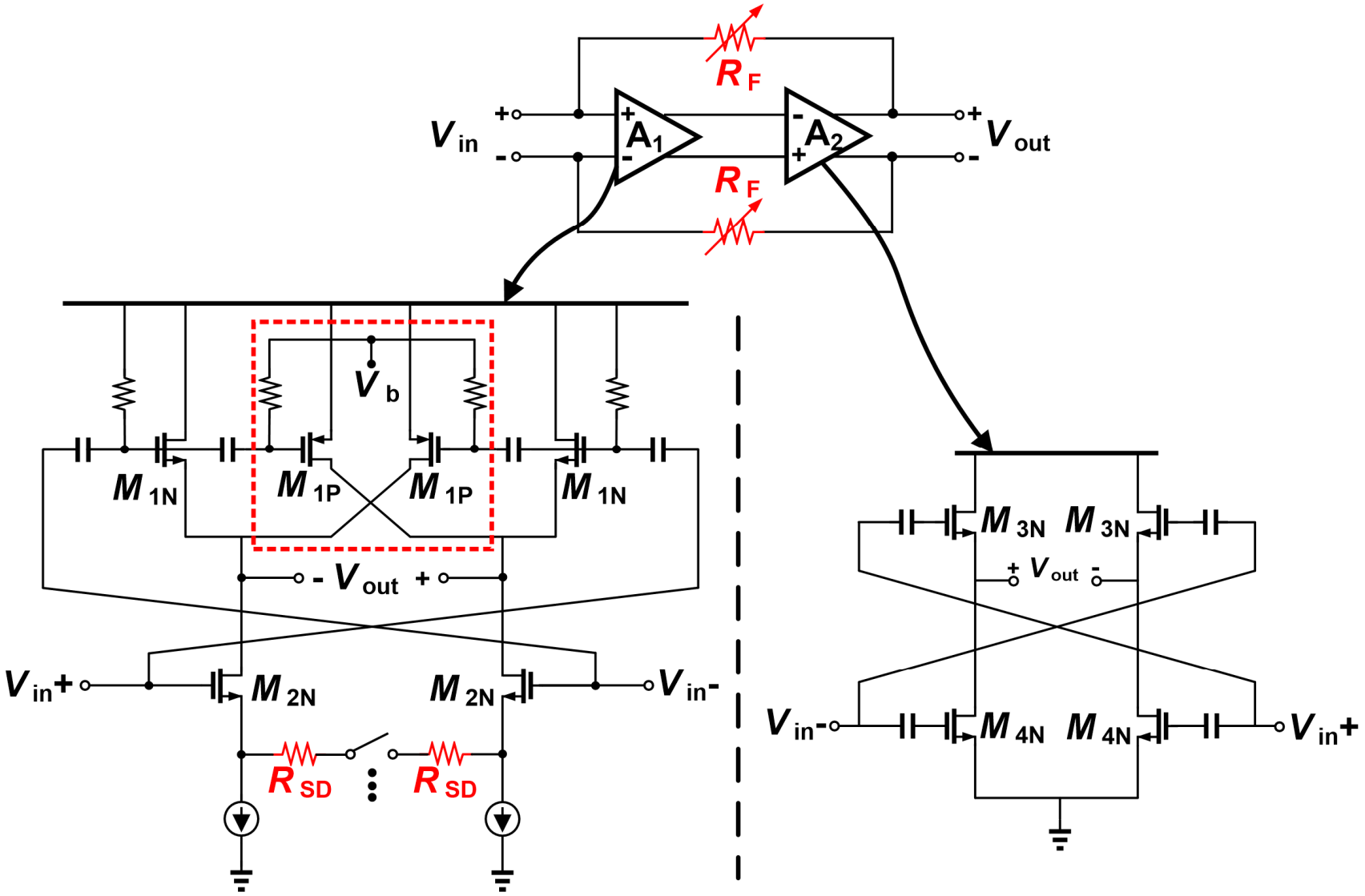
- I_{1P} is bleeded
- g_{m1N} can be reduced sustaining g_{m2N}
- Gain boosting

Even-order dist. suppression



- M_{1P} & M_{1N} →INV-type amp.
- Inherent even-order distortion suppression

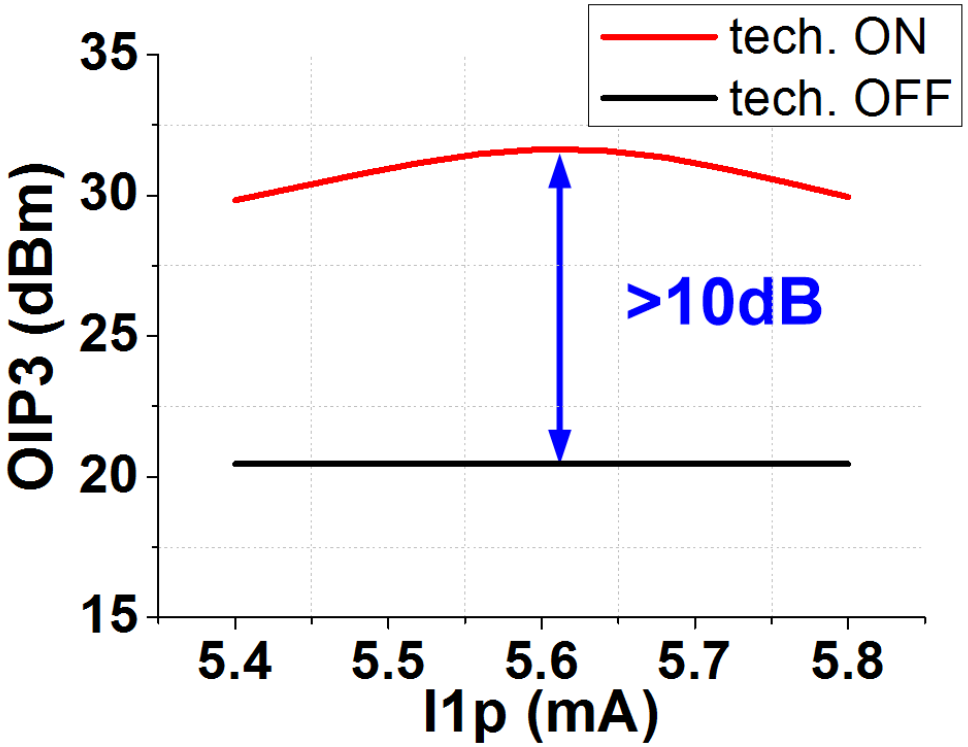
2-stage shunt FB WB-LNA



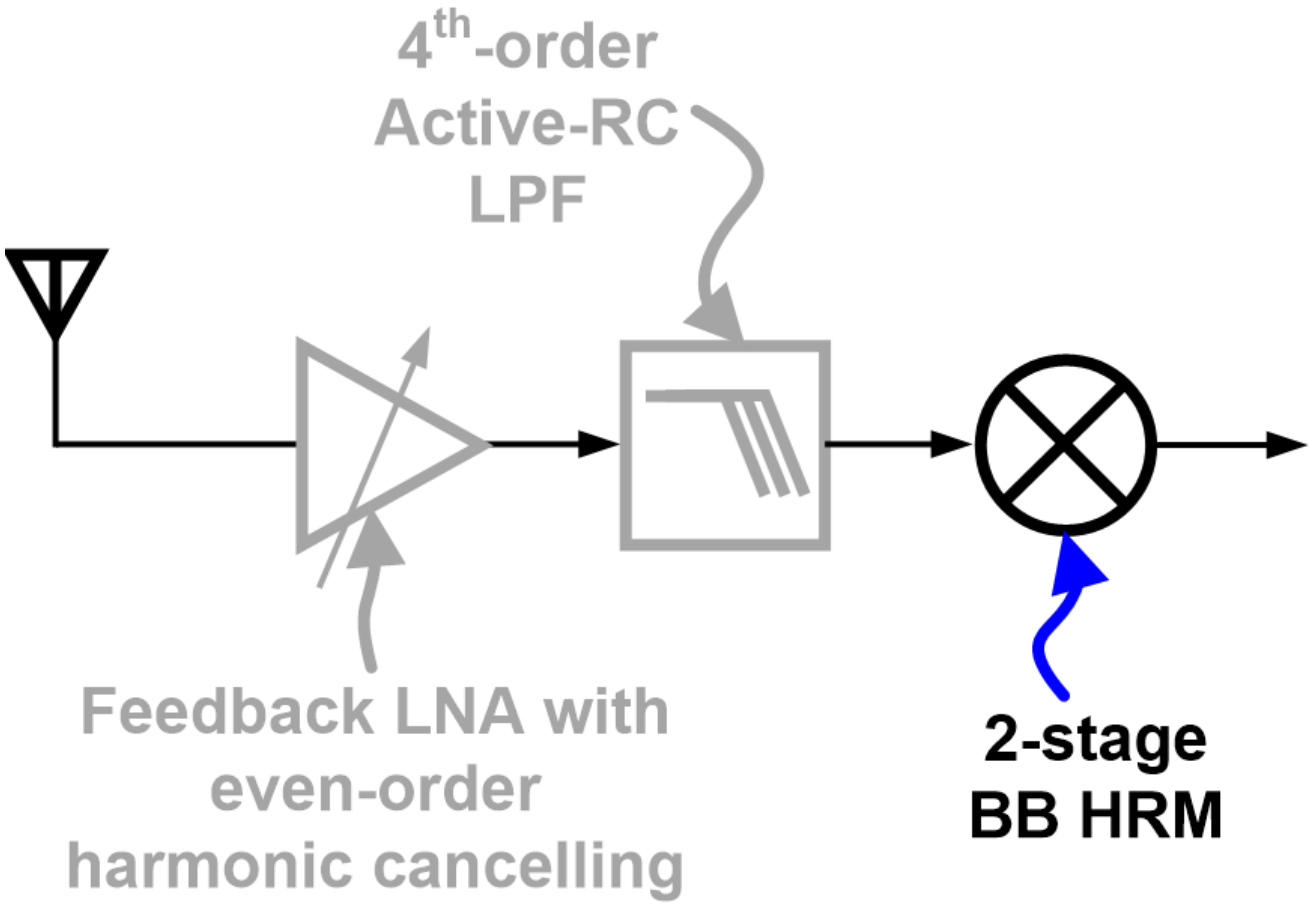
Linearity improvement

Parameter	gm			
	2nd-order	3rd-order	2nd-order Interaction	Higher order
Proposed	O	O	O	O

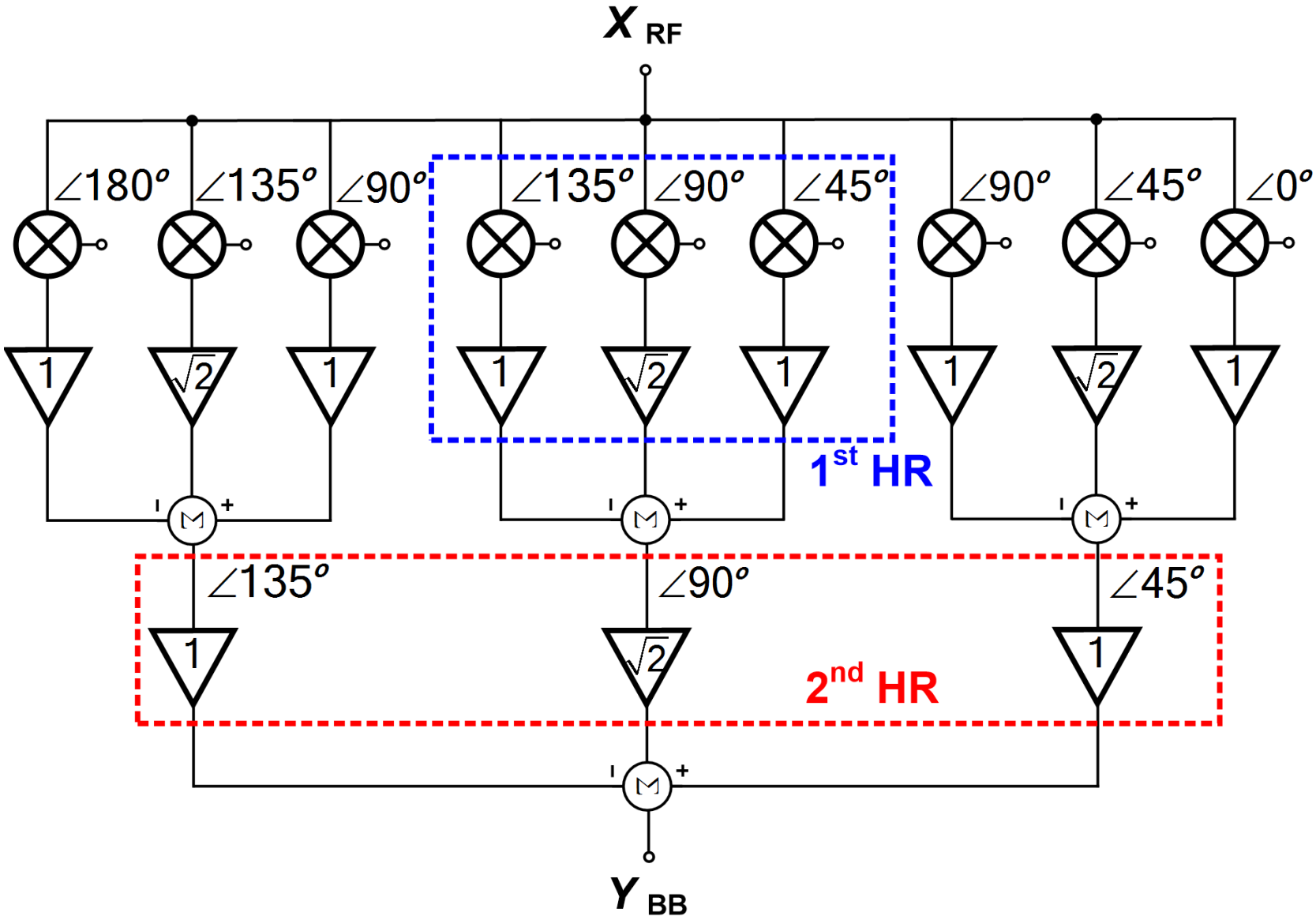
- Feedback
- Post nonlinearity correction
- G-boost & Even-order distortion supr. tech
- > 10dB improvement
- OIP3 reaches 31.8dBm



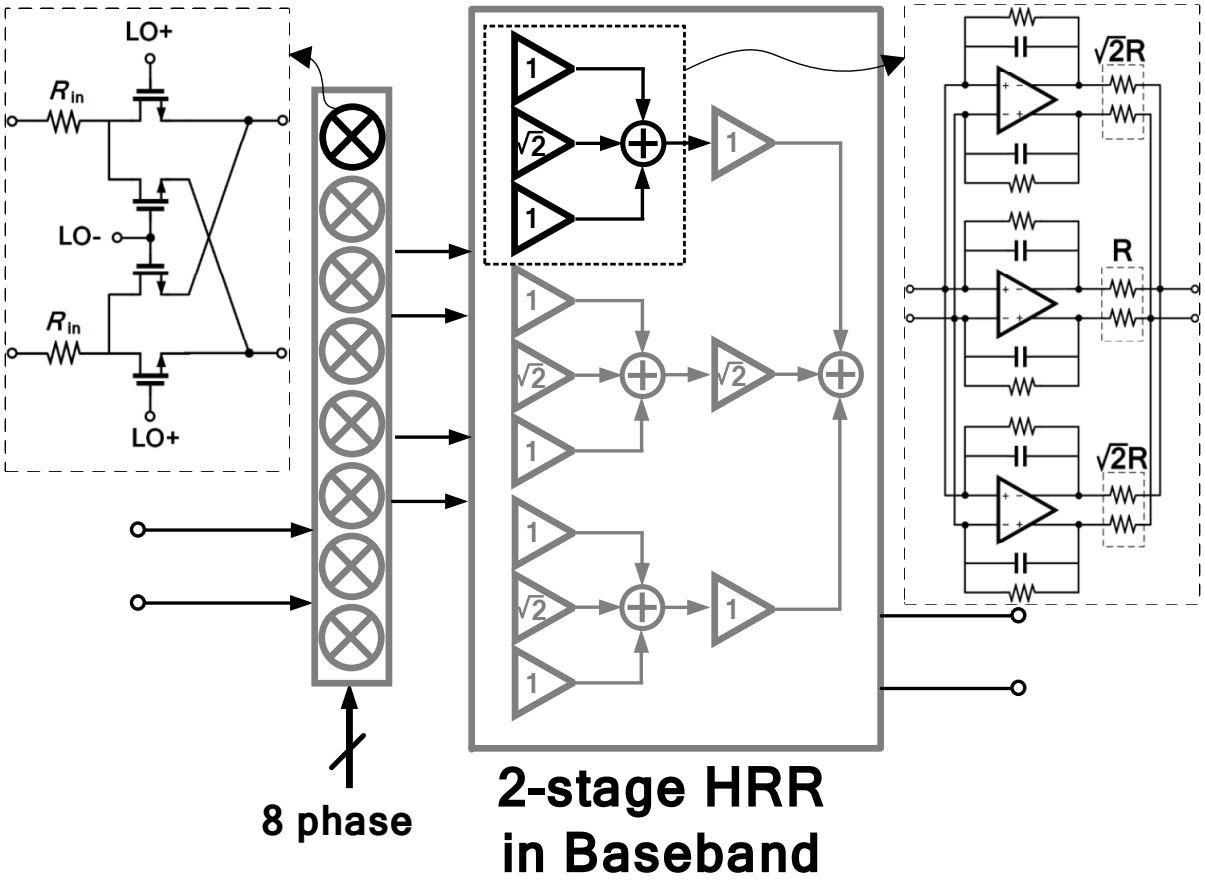
Highly linear TV tuner front-end [HRM]



2-stage baseband HR

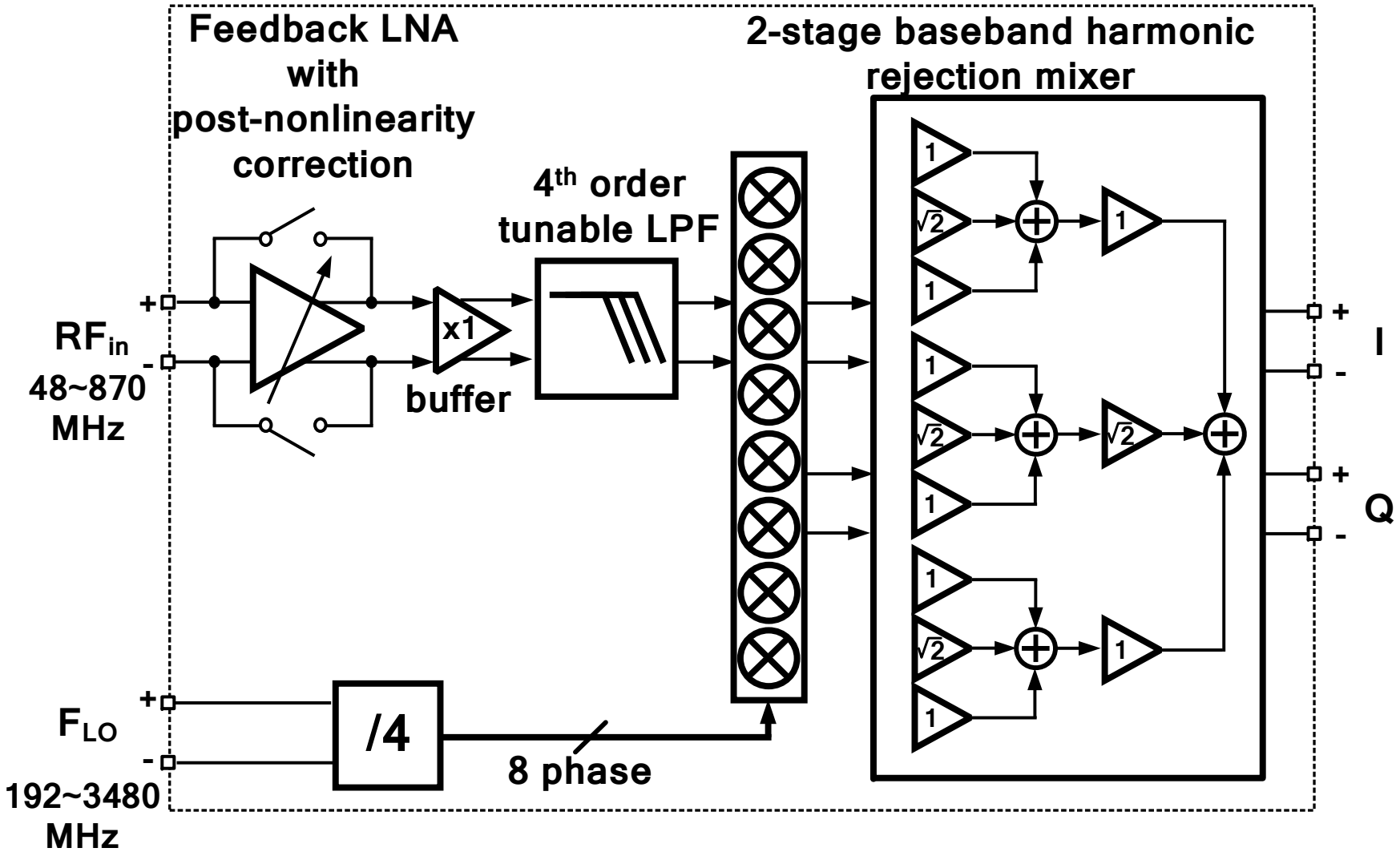


2-stage BB HRM

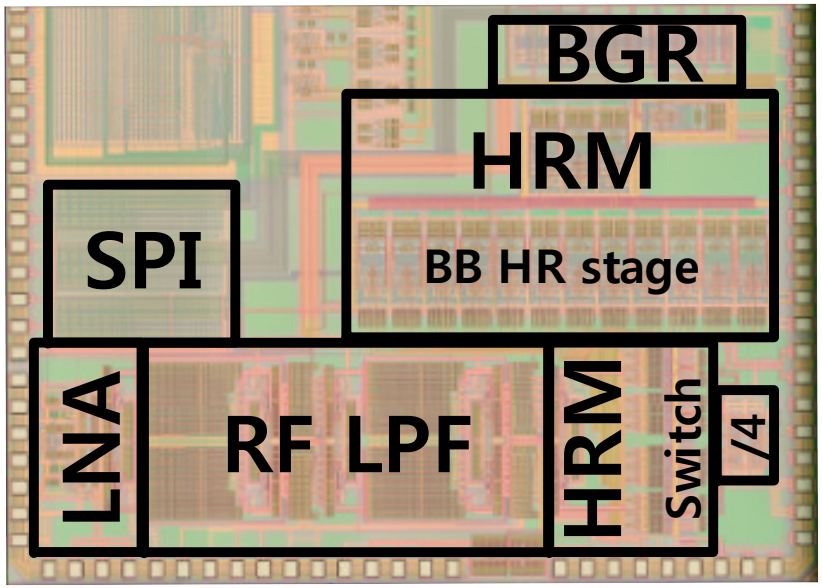


- 2-stage BB HR
- Performance
  - –G: 15 dB
  - –NF: 12 dB
  - –BW: 3~10MHz
  - –OIP3: 33dBm
  - –HRR3,5 > 60dB
  - –62mA / 1.5V [I,Q]

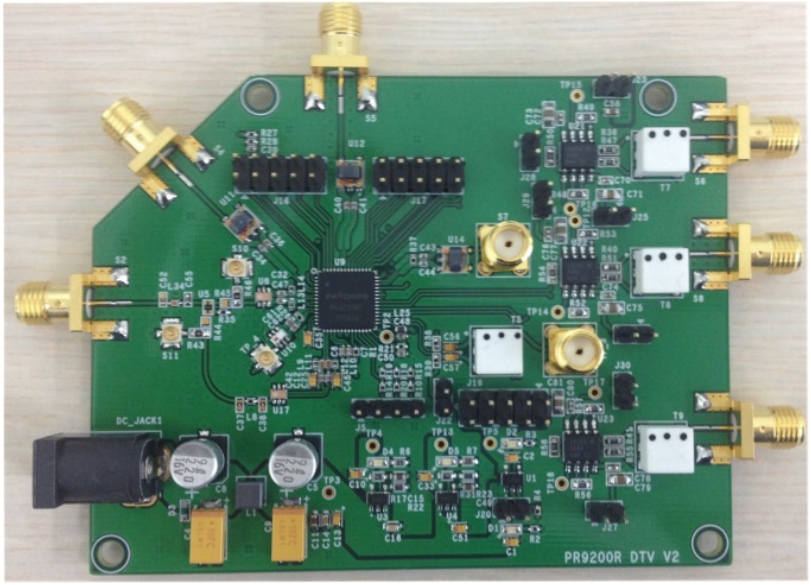
TV tuner front-end prototype



Implementation

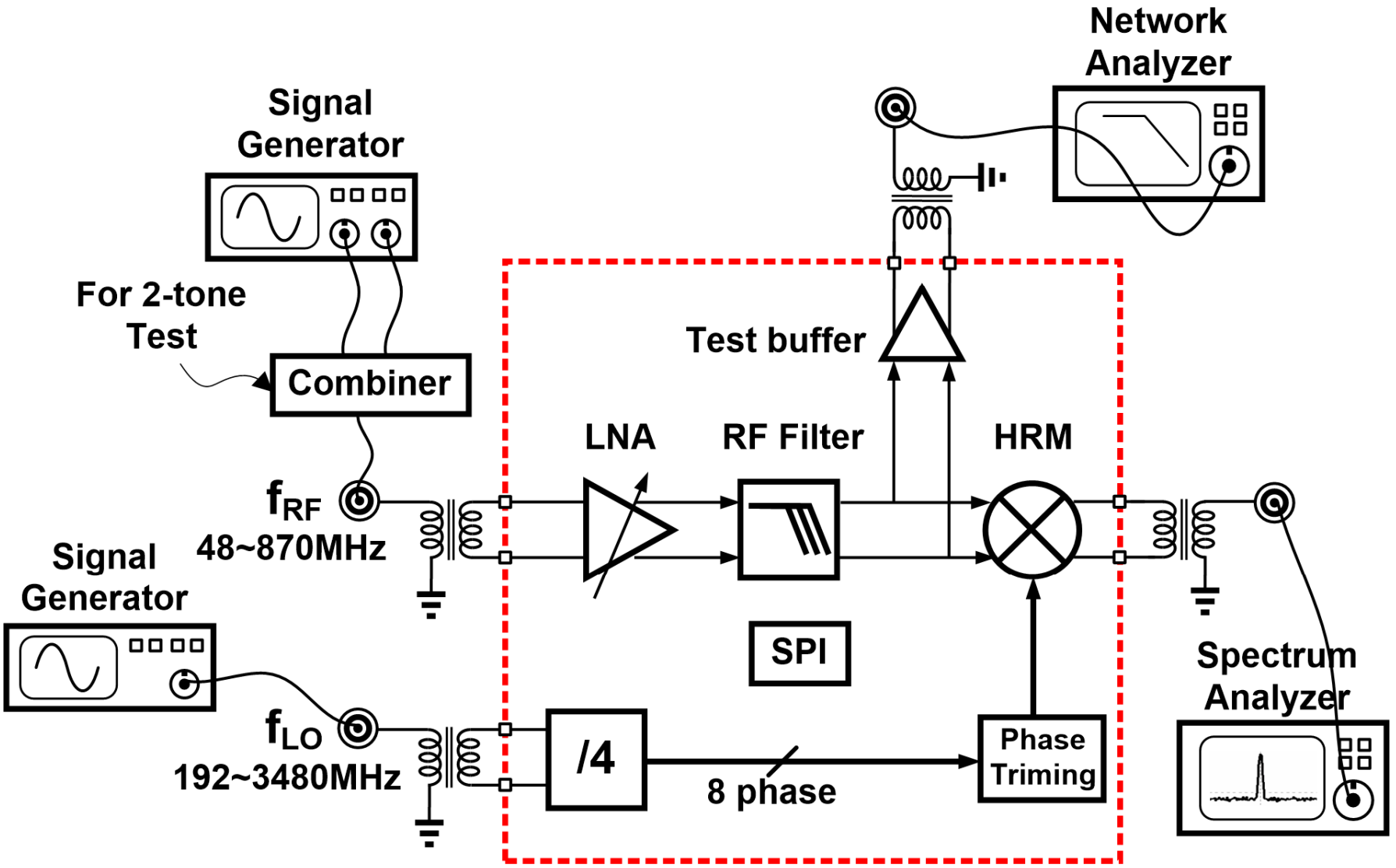


Chip micrograph (2.7mm^2)

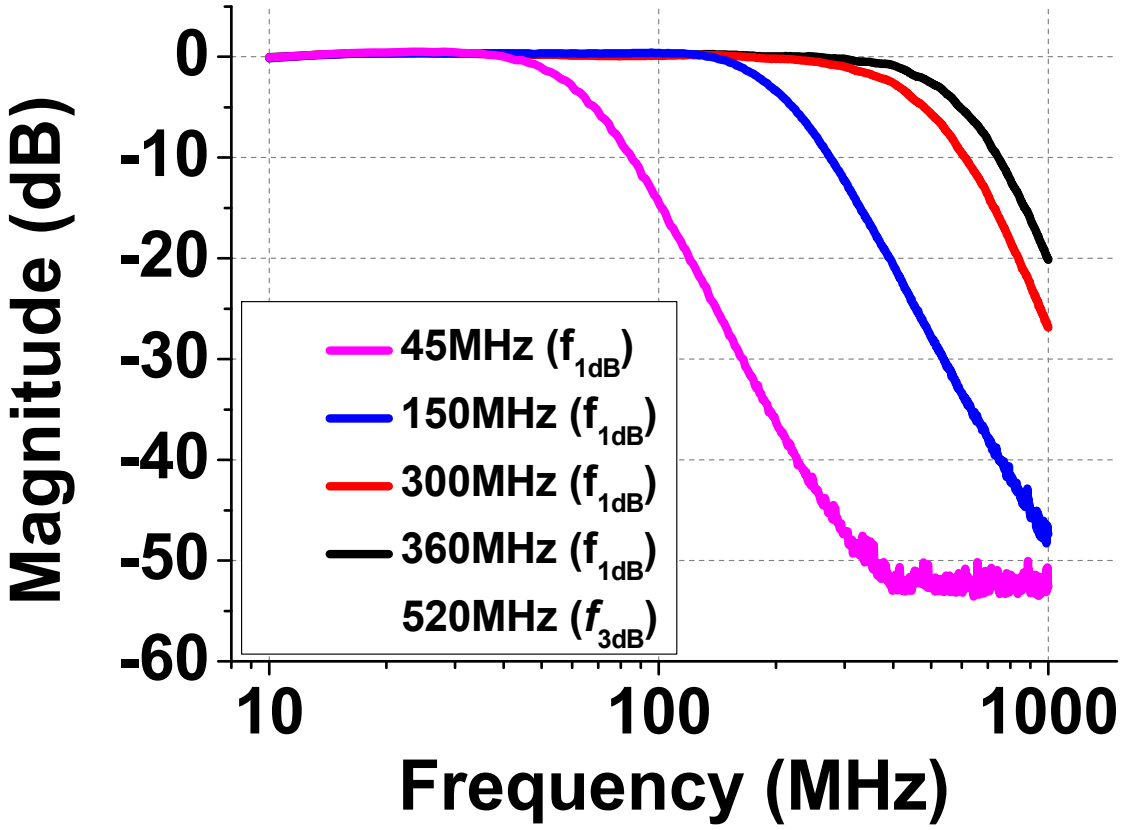


Test board

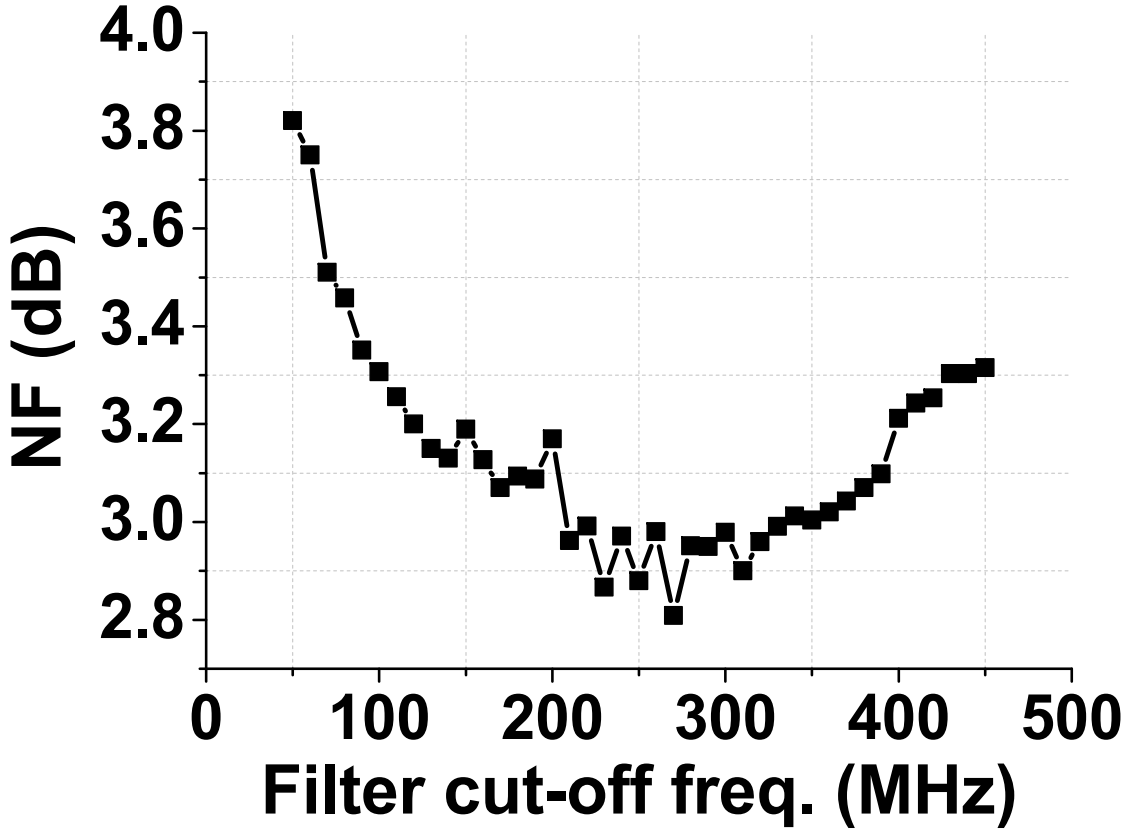
Measurement environment



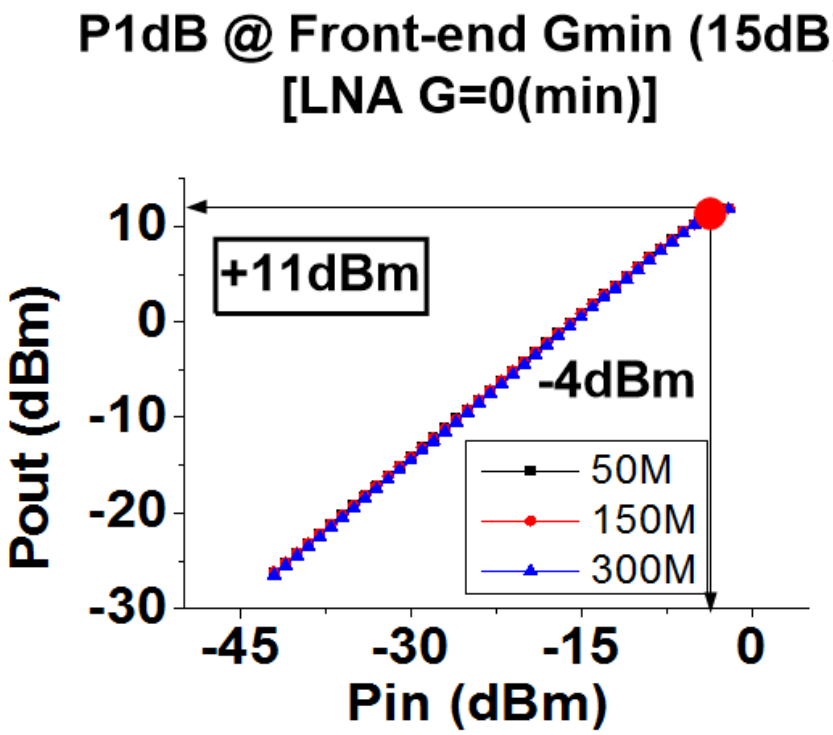
Measured filter frequency response

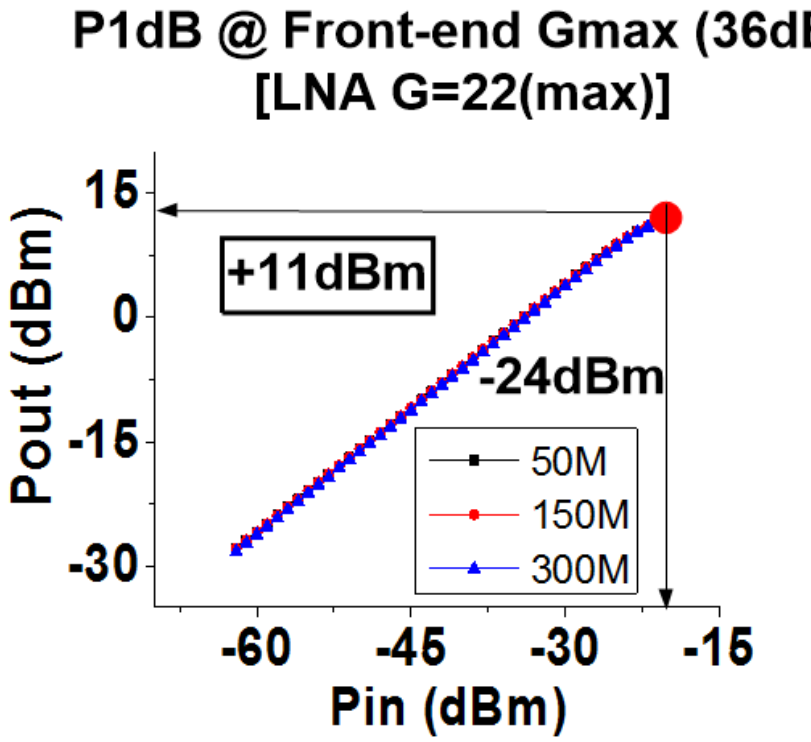


Measured front-end NF

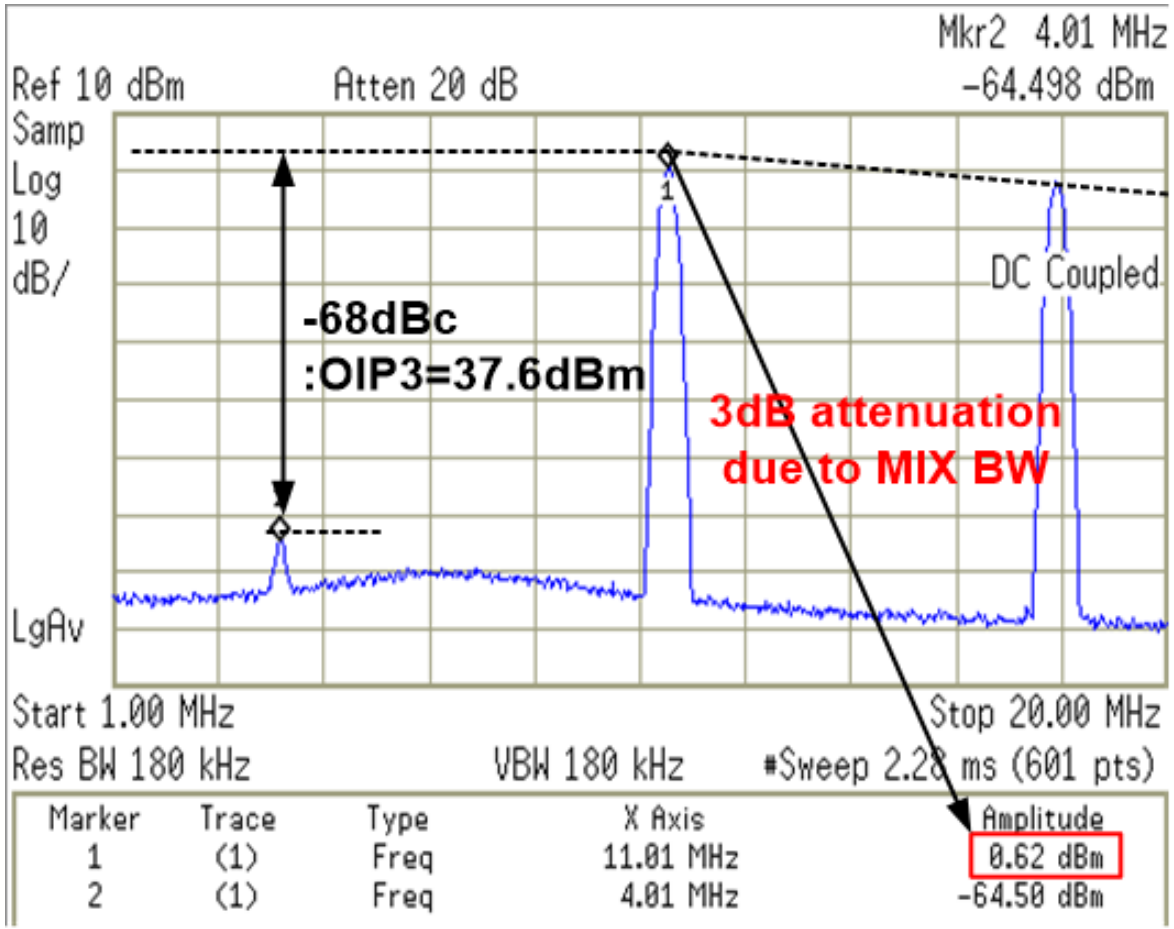


Measured P_{1dB} @$G_{min/max}$

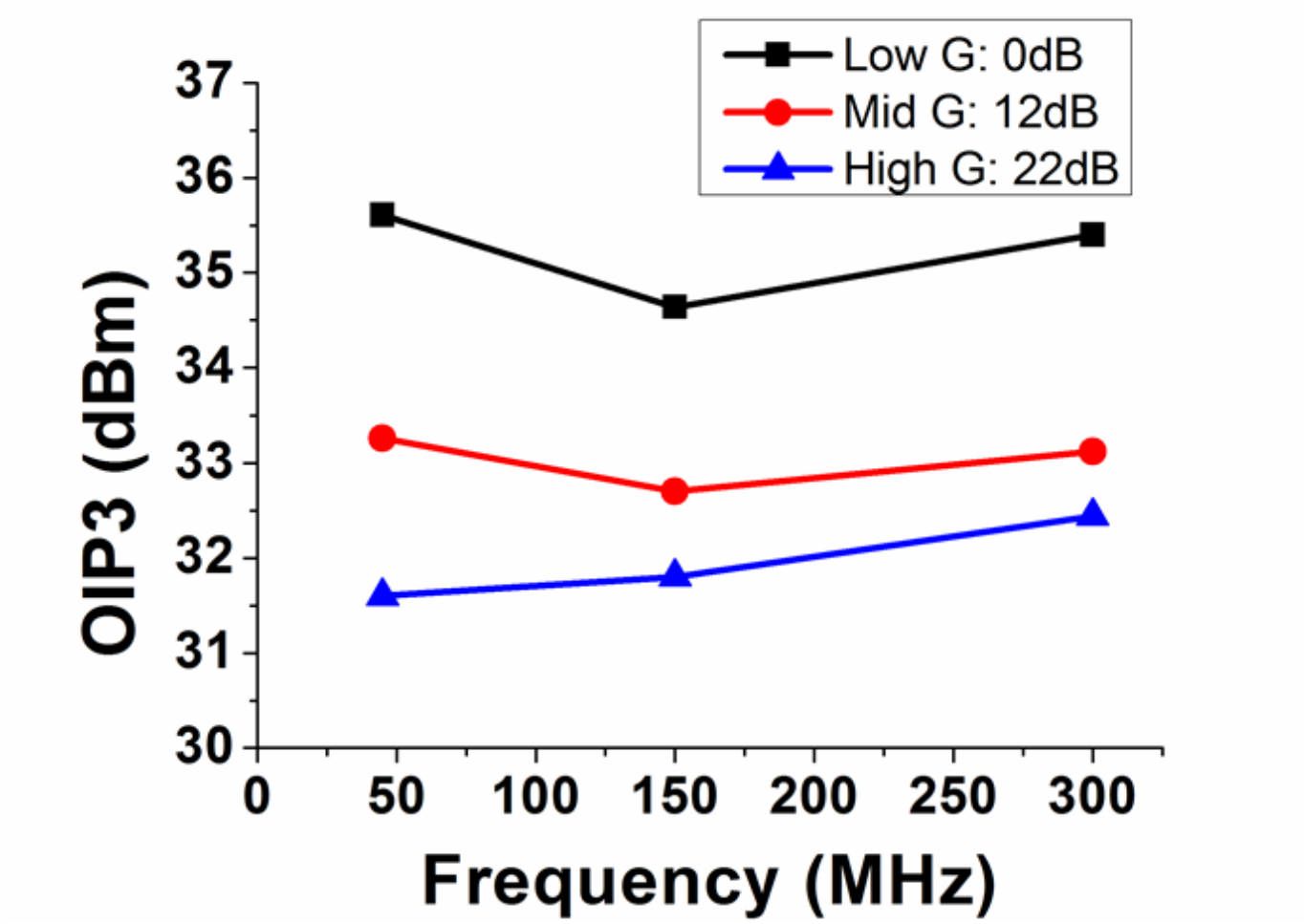




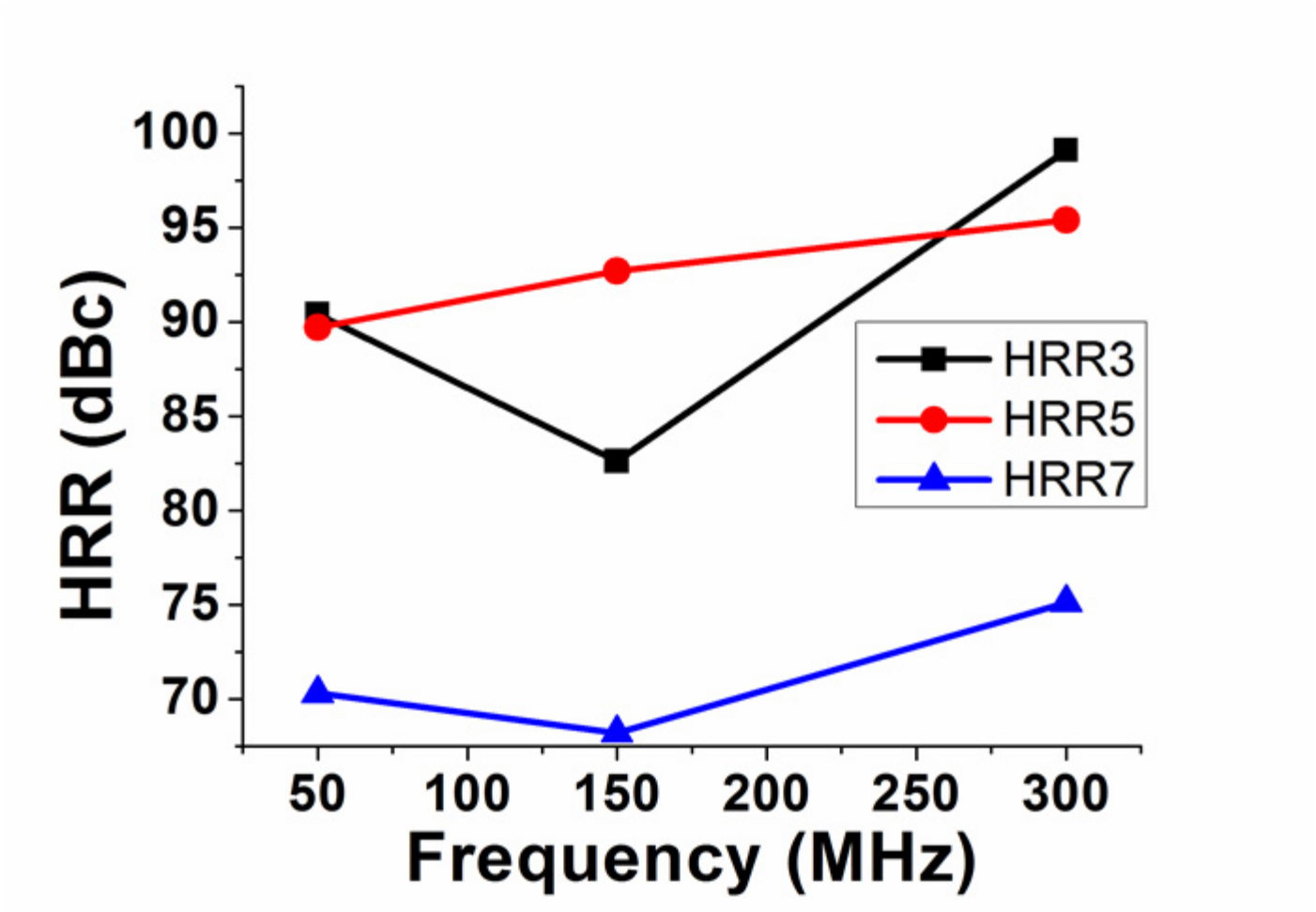
Measured IMD_3 @ MIX output



Measured front-end OIP_3



Measured harmonic rejection



Performance comparison

Parameter	T-MTT'10 Cha	JSSC'12 Im	JSSC'13 Choke	JSSC'13 Greenberg	**This work**
Front-End Gain max/min [dB]	+40/-22	+53/-26	+42/-36	+36/+15	**+36/+15**
NF@Gmax [dB]	5.5	6	5	3	**3.1**
OIP3 min/max [dBm]	+30/ N/A	+40/ N/A	+32.5/ N/A	+21/+30	**+31/+34**
OIP2 min/max [dBm]	N/A	N/A /+51	N/A /+62	+56/+66	**+59/+69**
Ext. IND in filter (#)	**Y(1)**	**Y(1)**	**Y(3)**	N	**N**
3rd HRR [dB]	>70	>70	>78	>65	**>83**
5th HRR [dB]	>70	>70	>84	>65	**>89**
7th HRR [dB]	>60	>65	N/A	>65	**>68**
Power [mW]	140* @1.8V	115* @1.5V	55* @1.5V	340** @1.8V	**183 @1.5V**
Technology	0.18um	0.18um	65nm	80nm	**0.13um**

*Ext. RF filter **All analog parts

Conclusion

- Fully integrated and state-of-the-art performance
  - G: (+15~36dB), NF: ~3.1dB, OIP3: >+31dBm, HRR3,5: >+83dB, HRR7: >+68dB
- >+25dBm IIP_3 RF LPF with sub-1-ohm Z_{out} SF
- Gain-boost and Even-order distortion suppression tech. in LNA
- 2-stage baseband harmonic rejection robust to gain-mismatch

Acknowledgement

- National Research Foundation for funding
- PHYCHIPS for chip fabrication

- Seung-Min Oh
- Dae-Yeon Kim
- Jong-Kyung Lee

A Fully Integrated Highly Reconfigurable Discrete-Time Super-Heterodyne Receiver

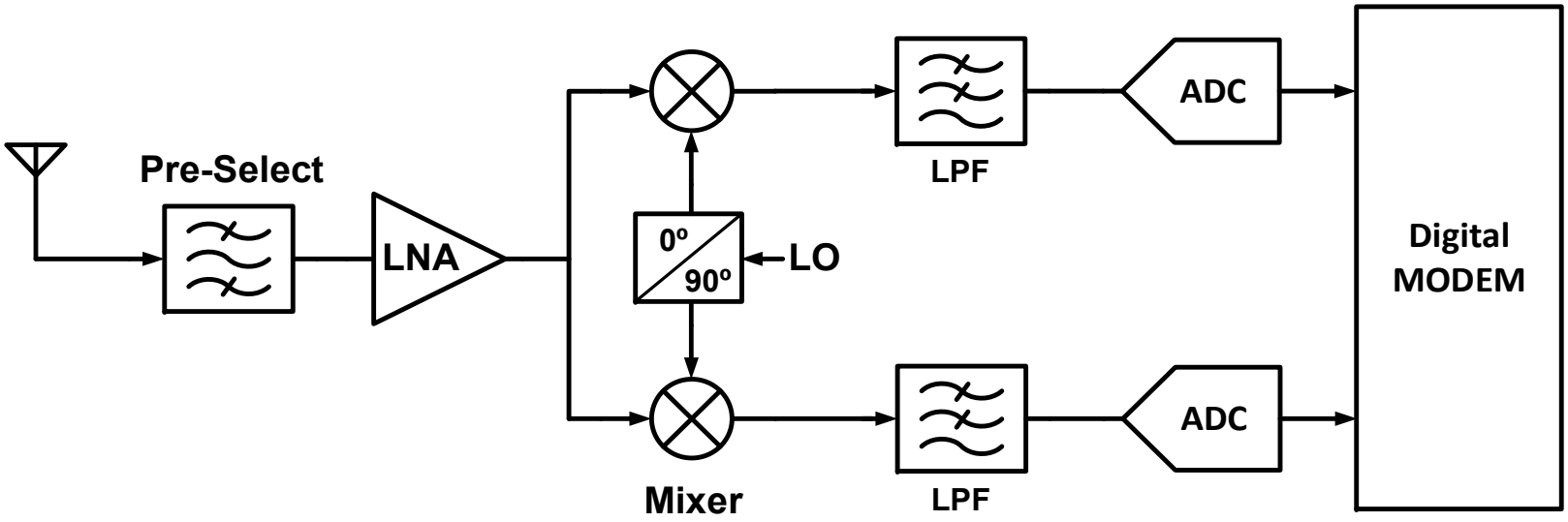
Massoud Tohidian
Iman Madadi
R. Bogdan Staszewski

TU Delft
Delft University of Technology

Outline

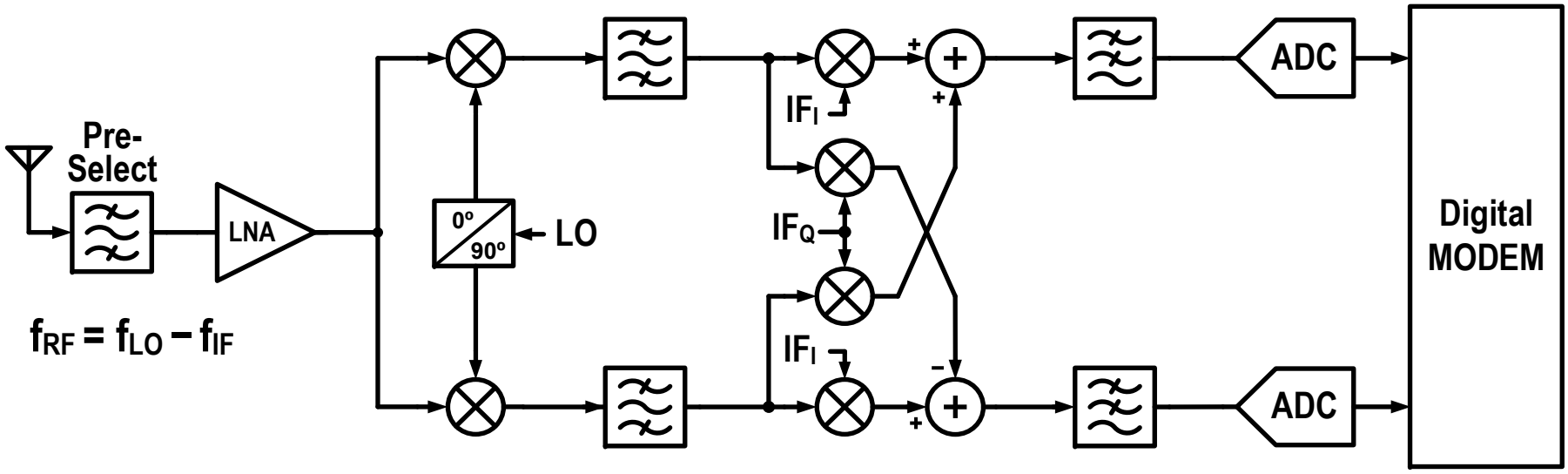
- Introduction
- Sampling in DT receivers
- Proposed super-heterodyne structure
  - 4x sampling concept
  - I/Q charge-sharing complex BPF
  - Noise cancelling LNTA
- Measurement results
- Conclusion

Zero/Low-IF Receiver



- ✓ Highly integrated
- ✓ No image problem
- ✘ 2nd-order nonlinearity
- ✘ LO self mixing
- ✘ Flicker noise

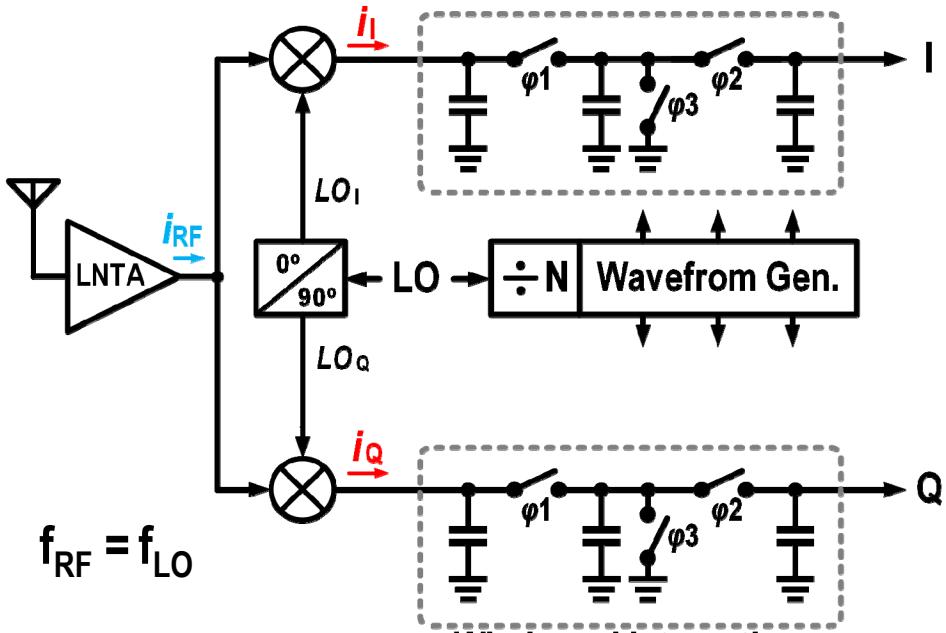
Super-Heterodyne Receiver

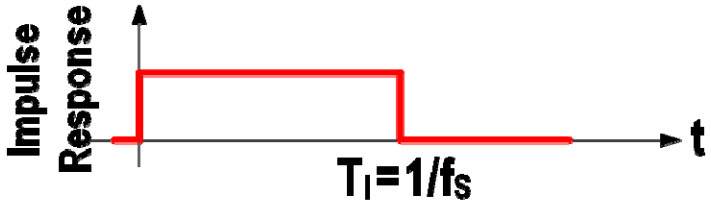


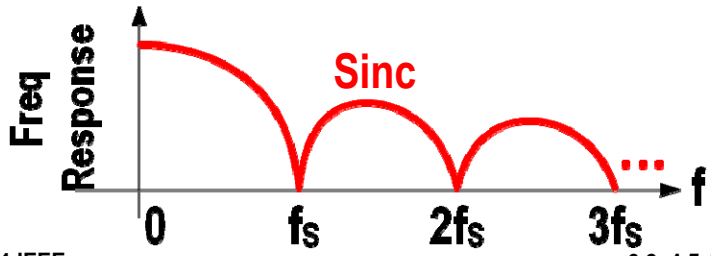
- ✓ Very high IIP2
- ✓ Flicker free gain at IF
- ✓ LO self mixing solved
- ! Image frequency
- ! Integration of BPF

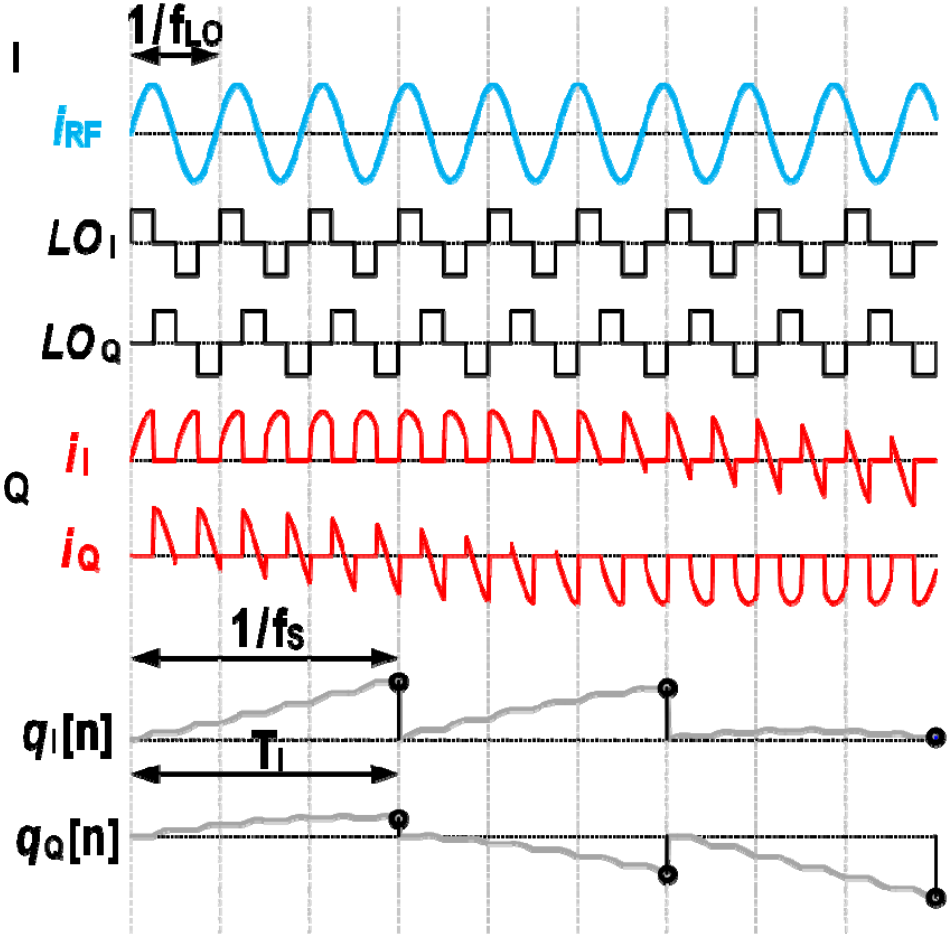
[Mirzaei ISSCC'11]
[Madadi RFIC'13]

Discrete-Time Zero-IF Receiver



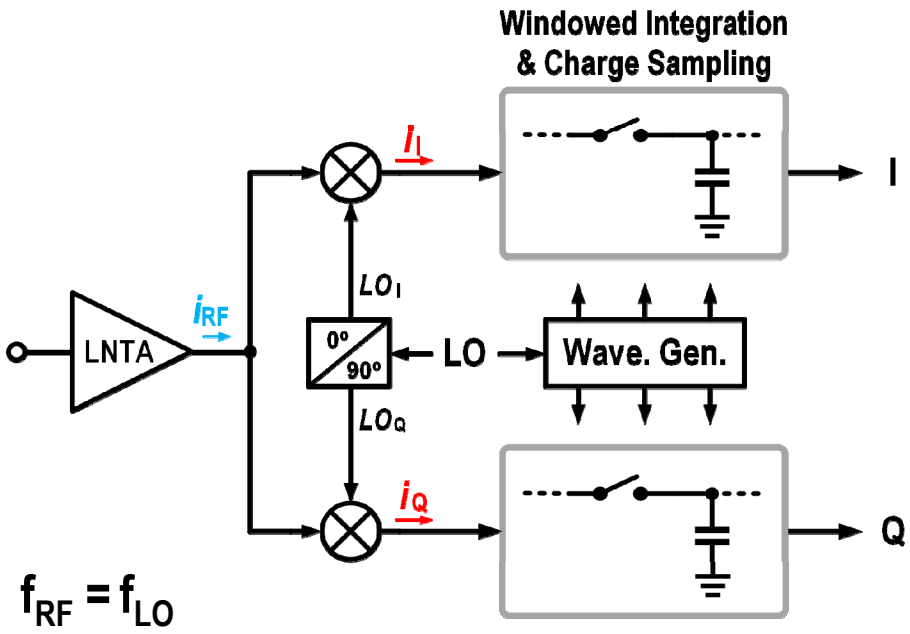


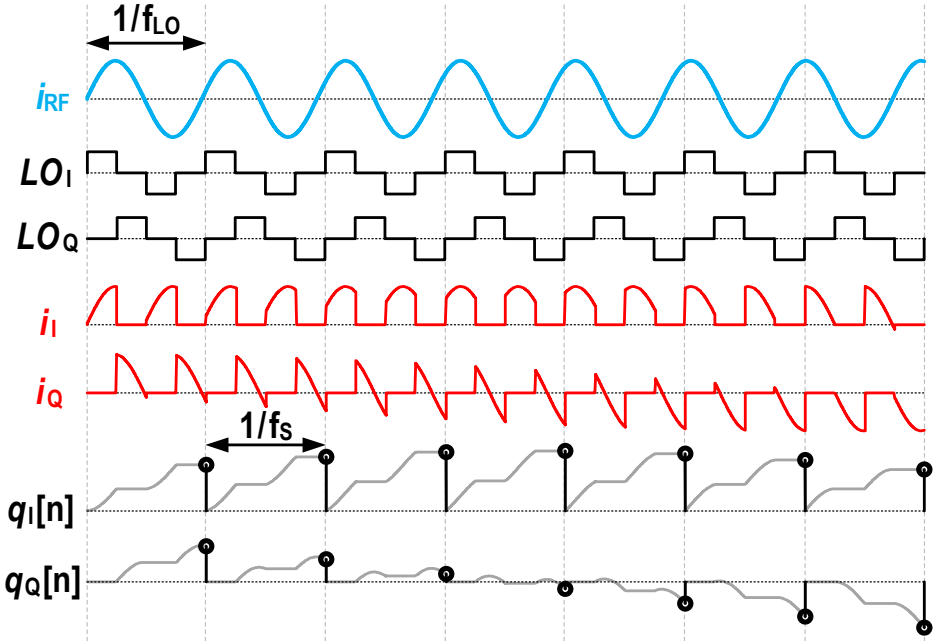


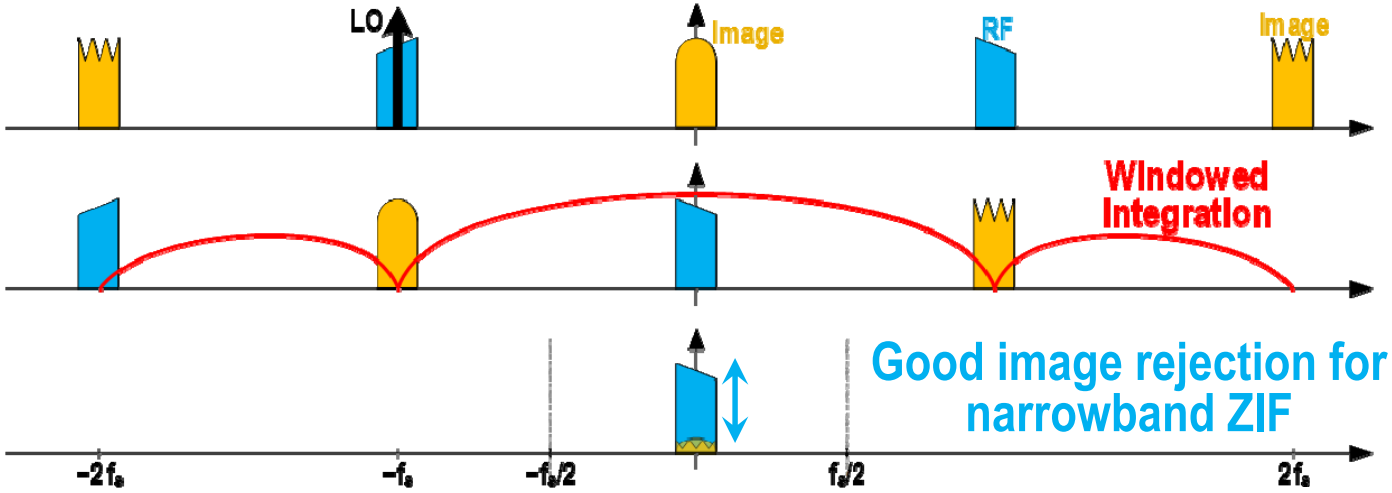


Low output data rate

1x Sampling in DT Zero-IF RX

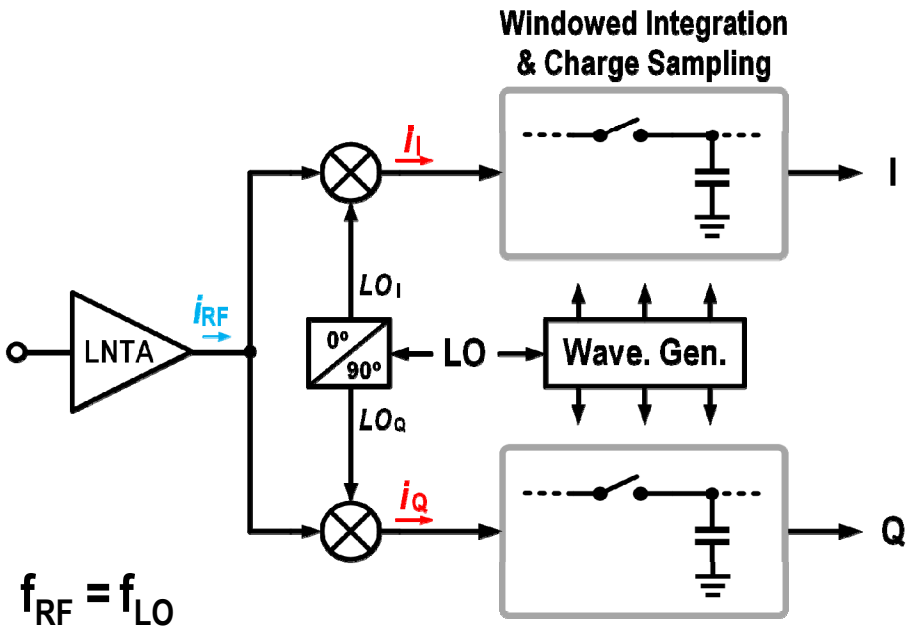


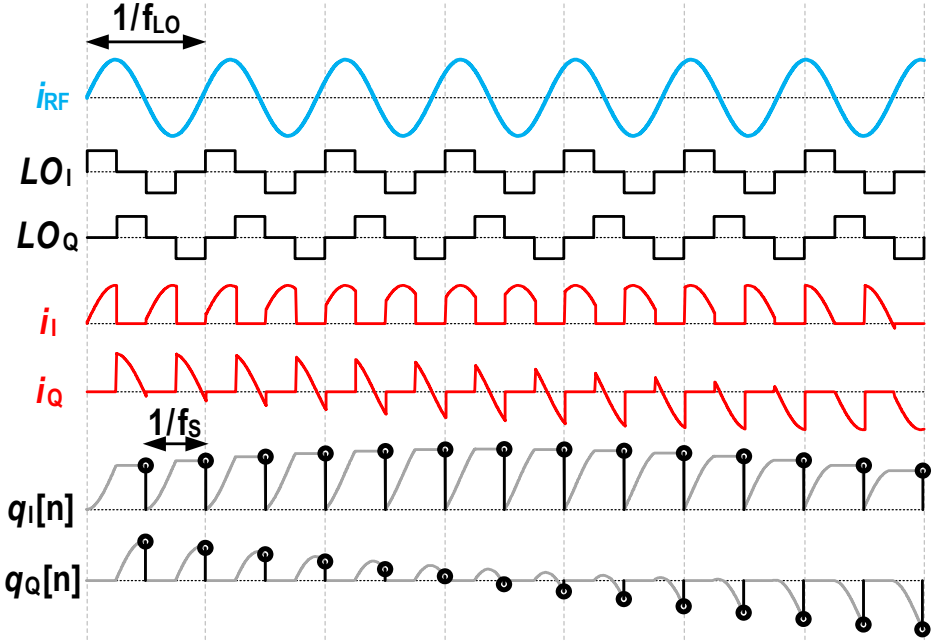


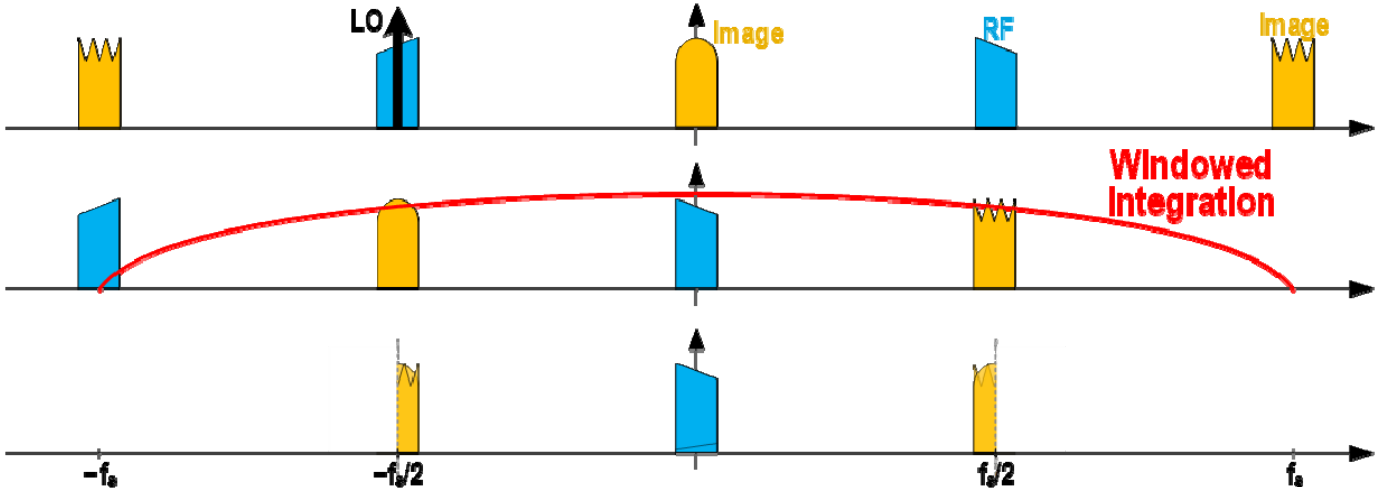


[Bagheri JSSC'05]

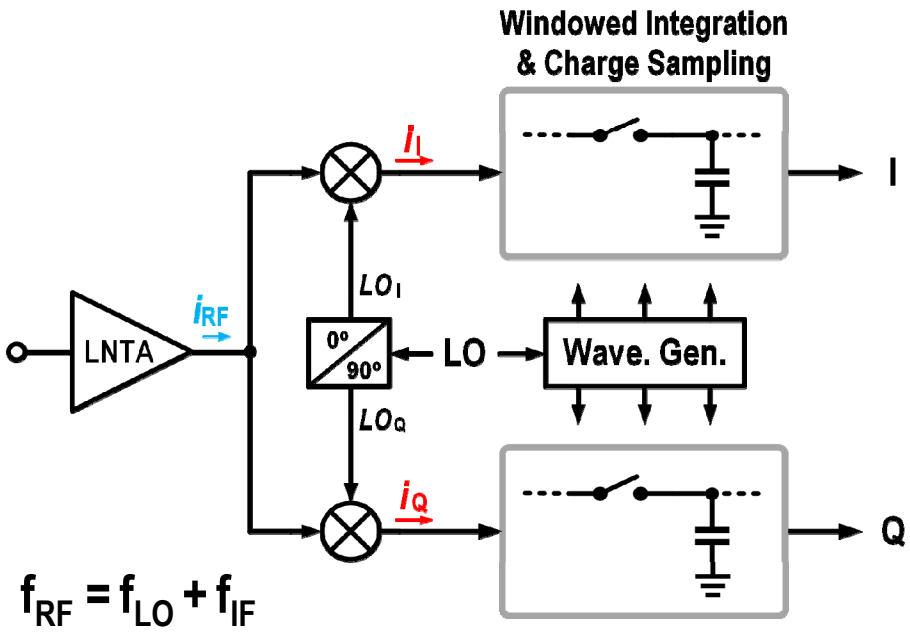
2x Sampling in DT Zero-IF RX

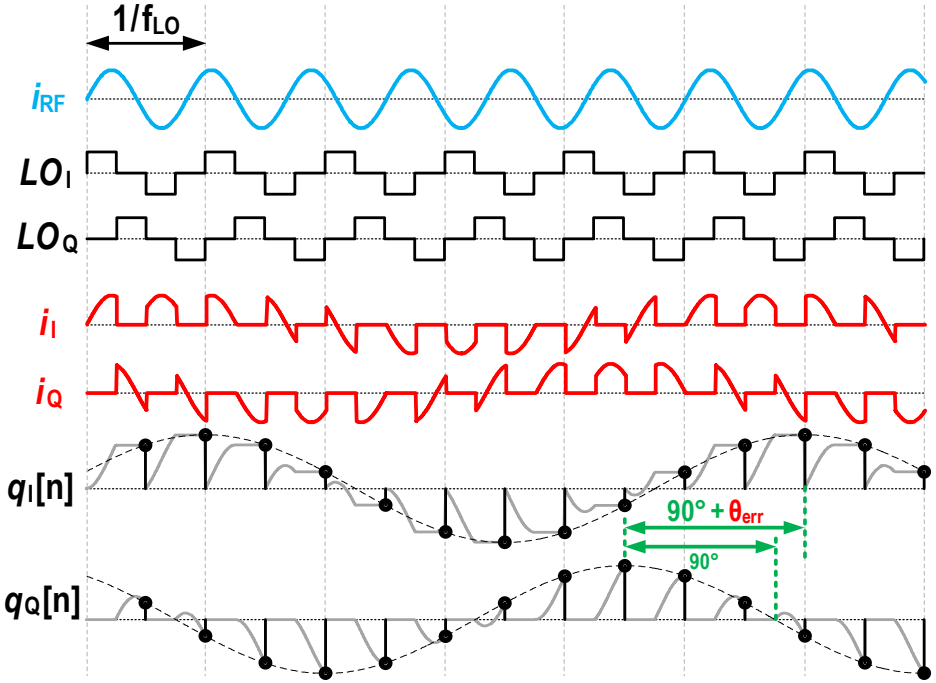


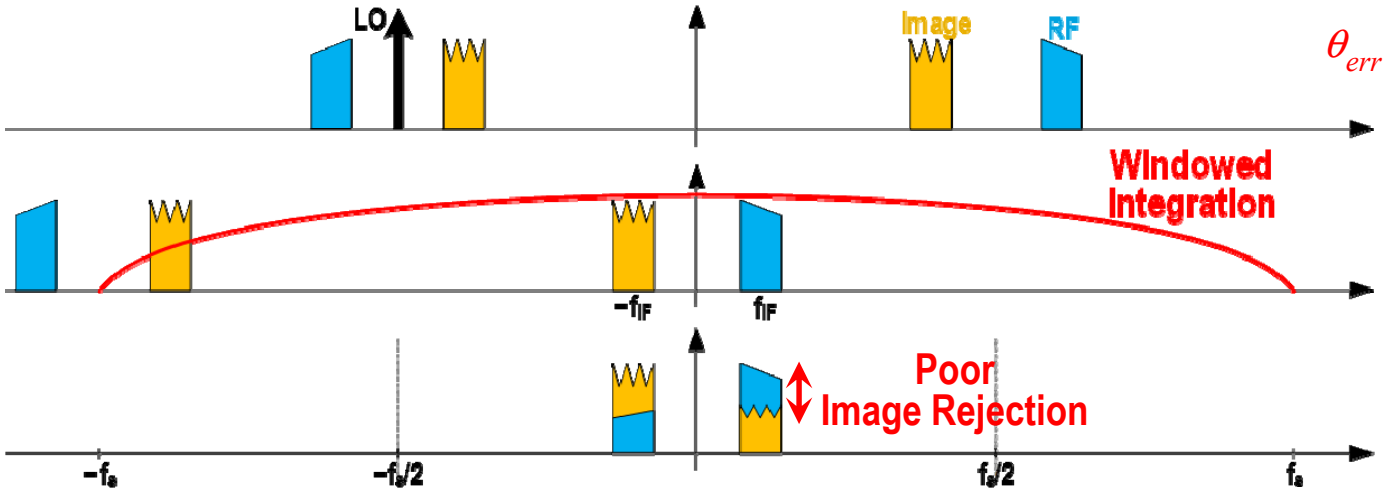




2x Sampling in DT High-IF RX

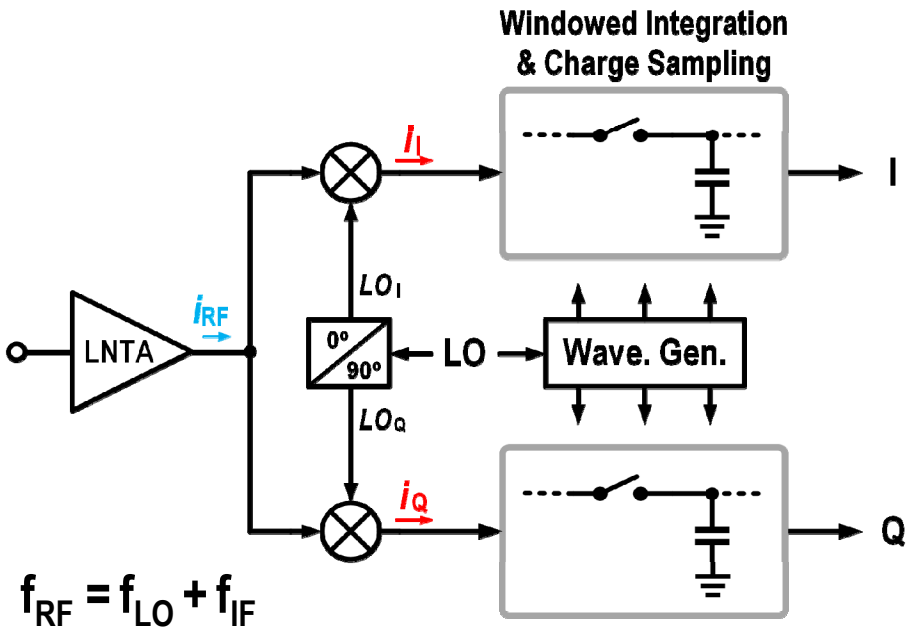


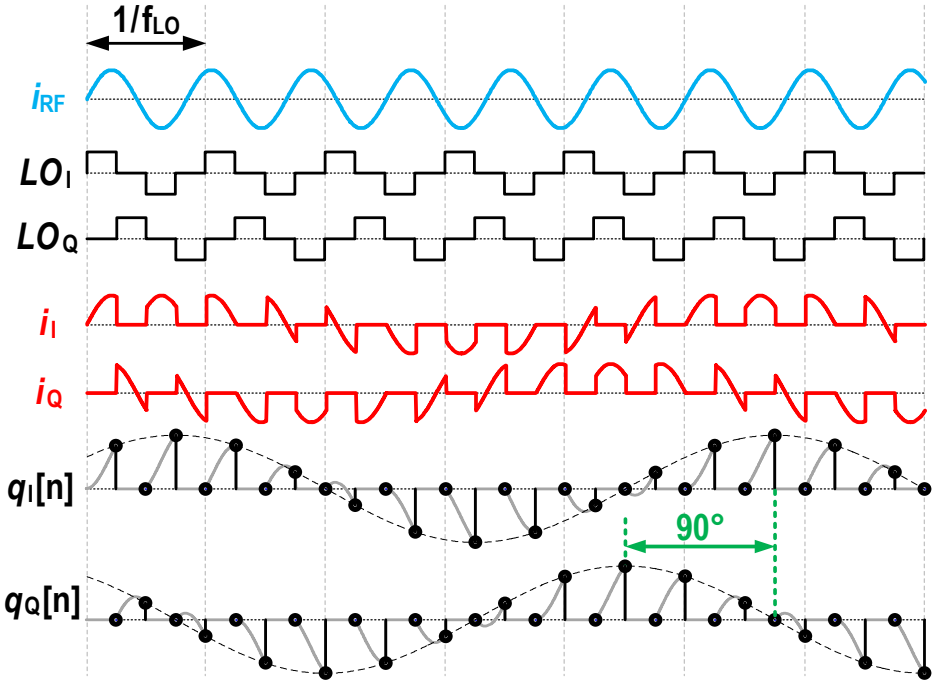


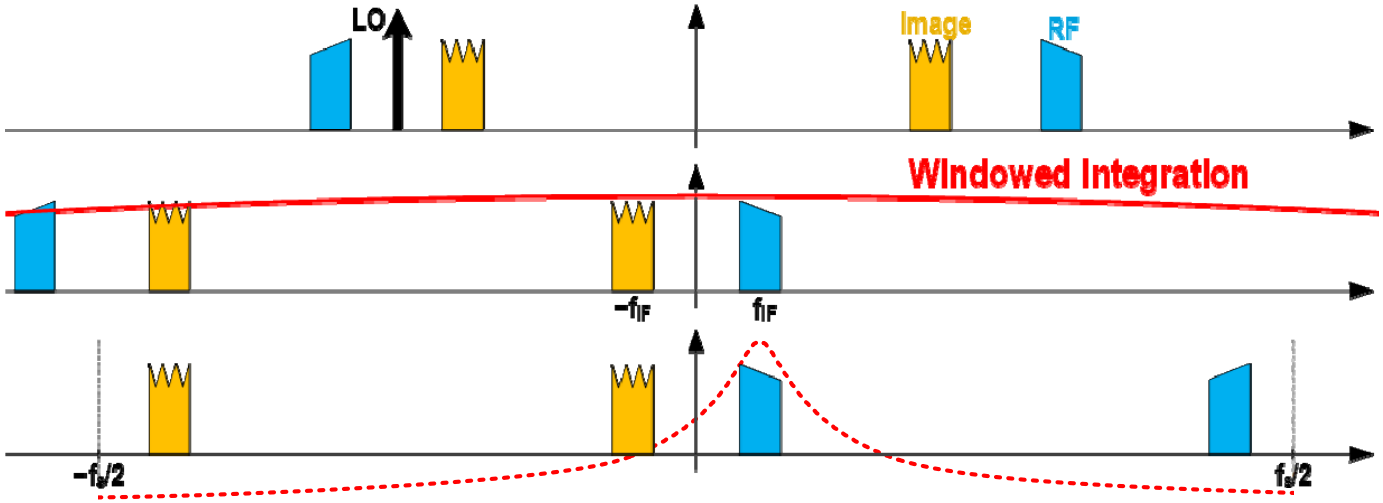


$$\theta_{err} = \frac{T_s}{2} \times 2\pi f_{IF}$$

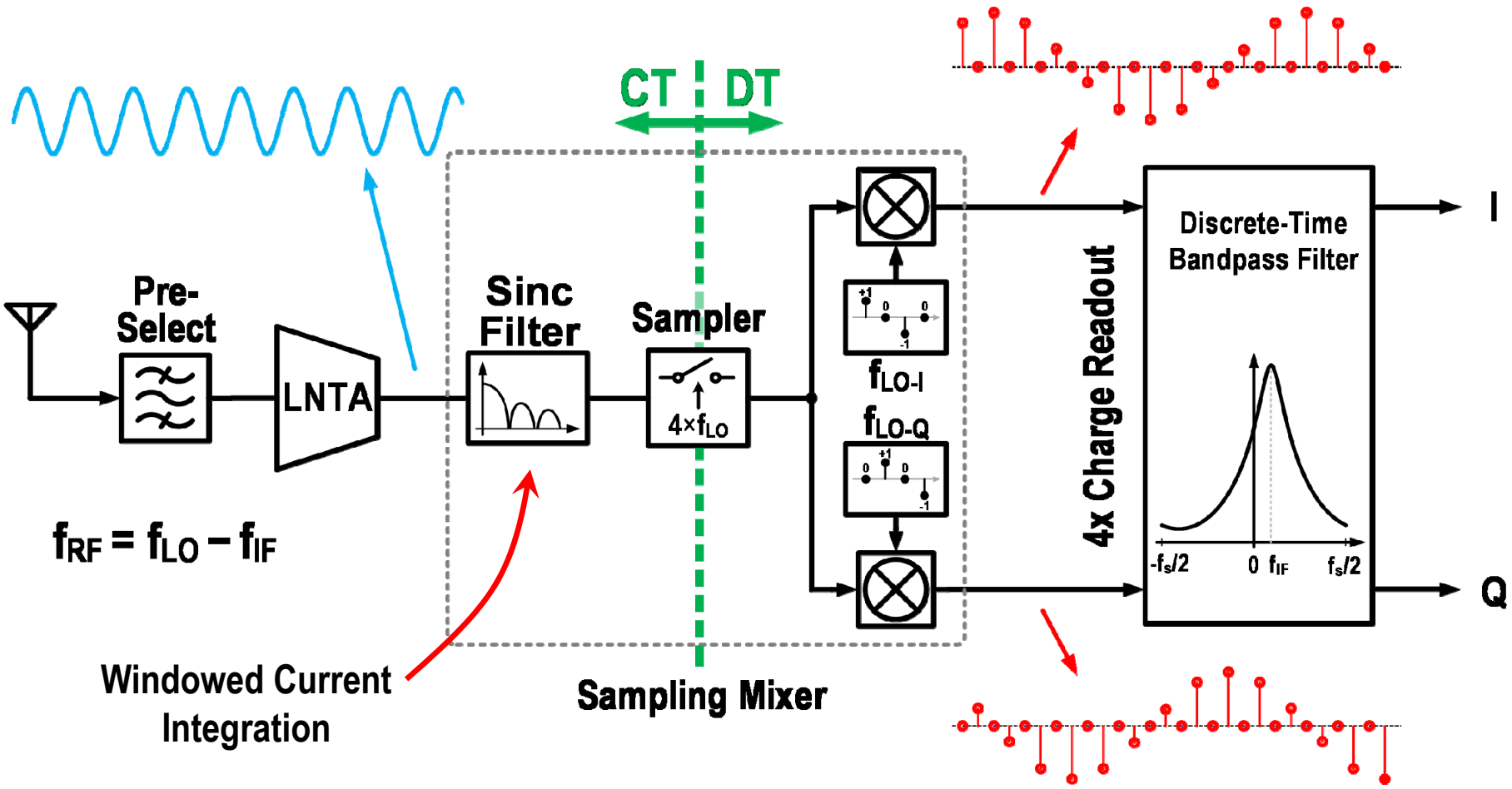
Proposed 4x Sampling for High-IF RX







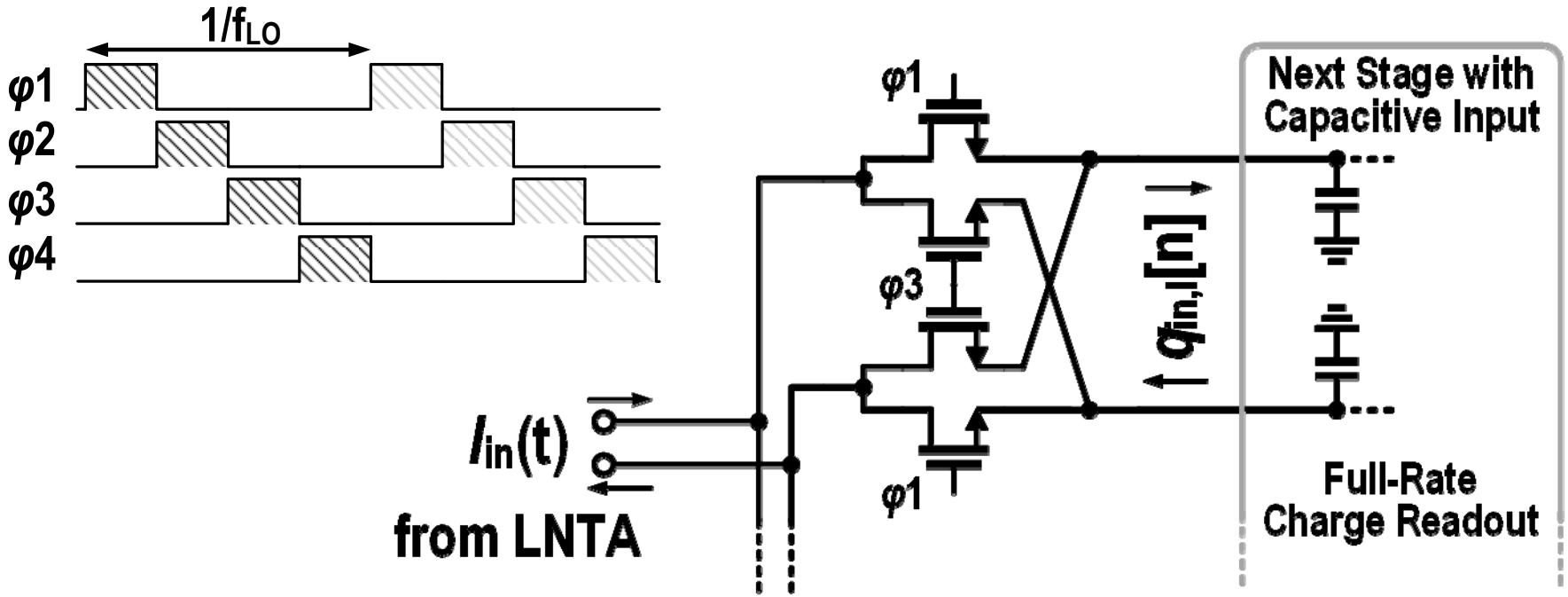
Proposed 4x Sampling for High-IF RX



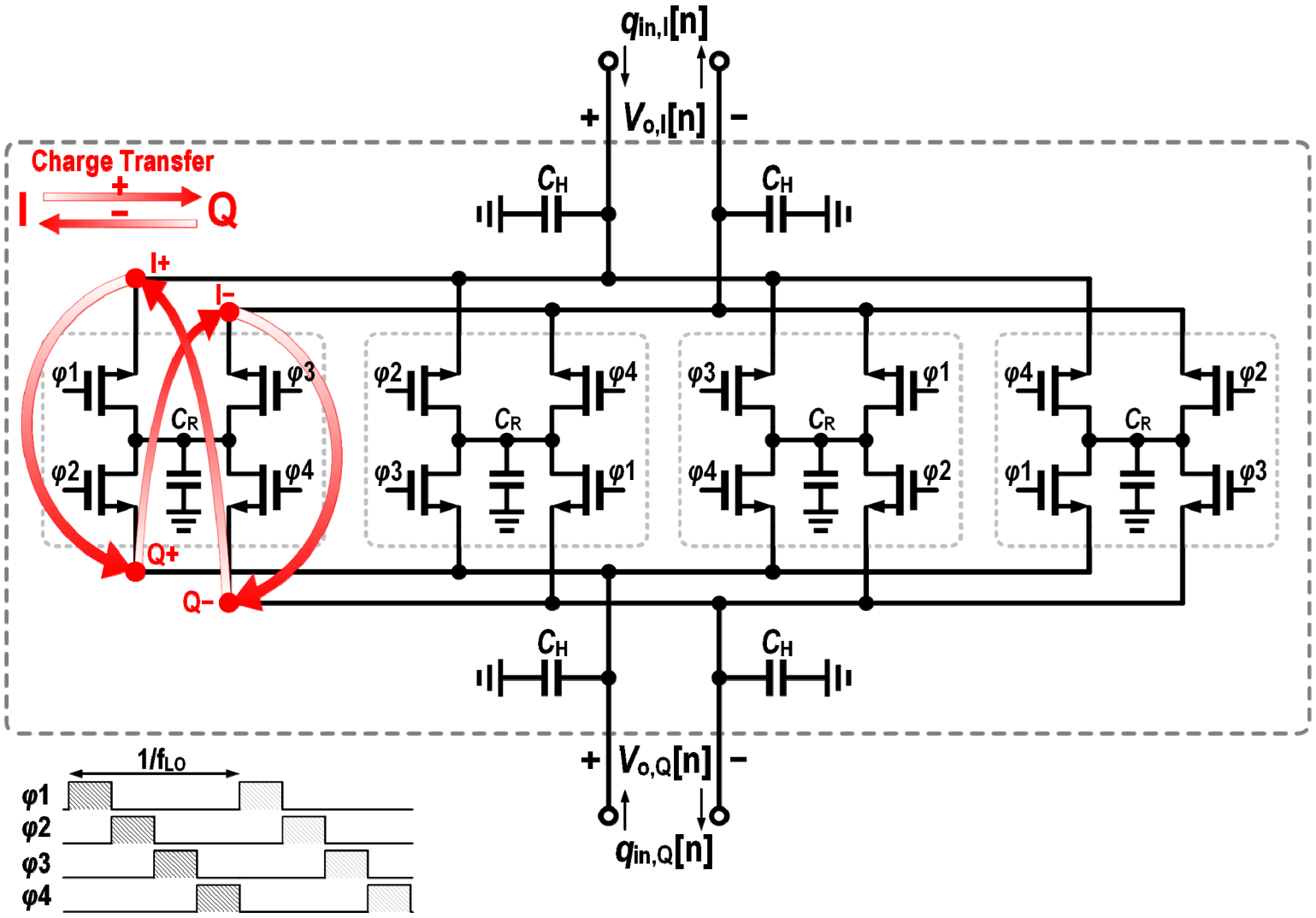
More than 10GS/s

Sampling Mixer

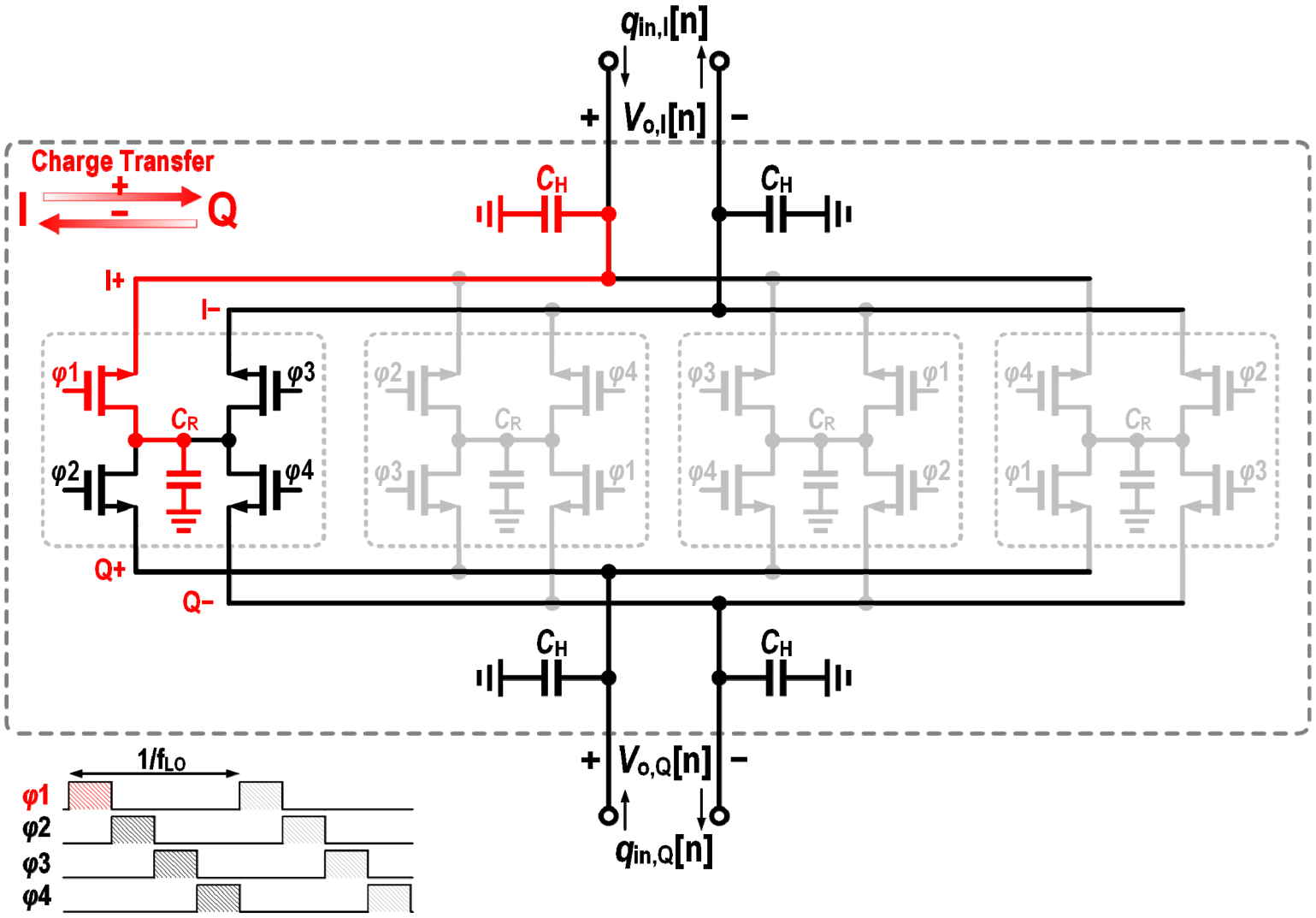
- Passive mixer
  - Both sampling and DT mixing
- Input current → sampled charge



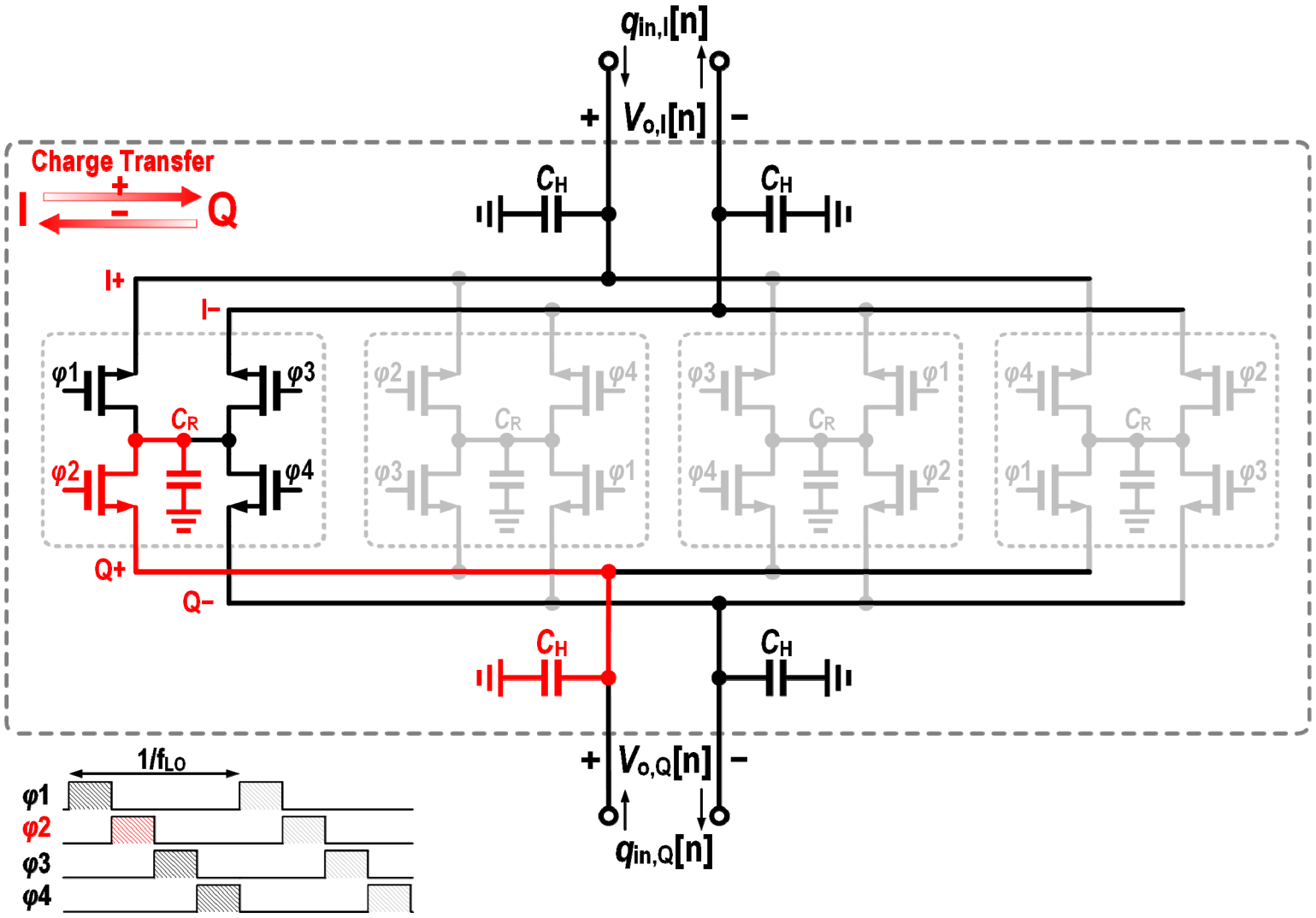
I/Q Charge-Sharing Complex BPF



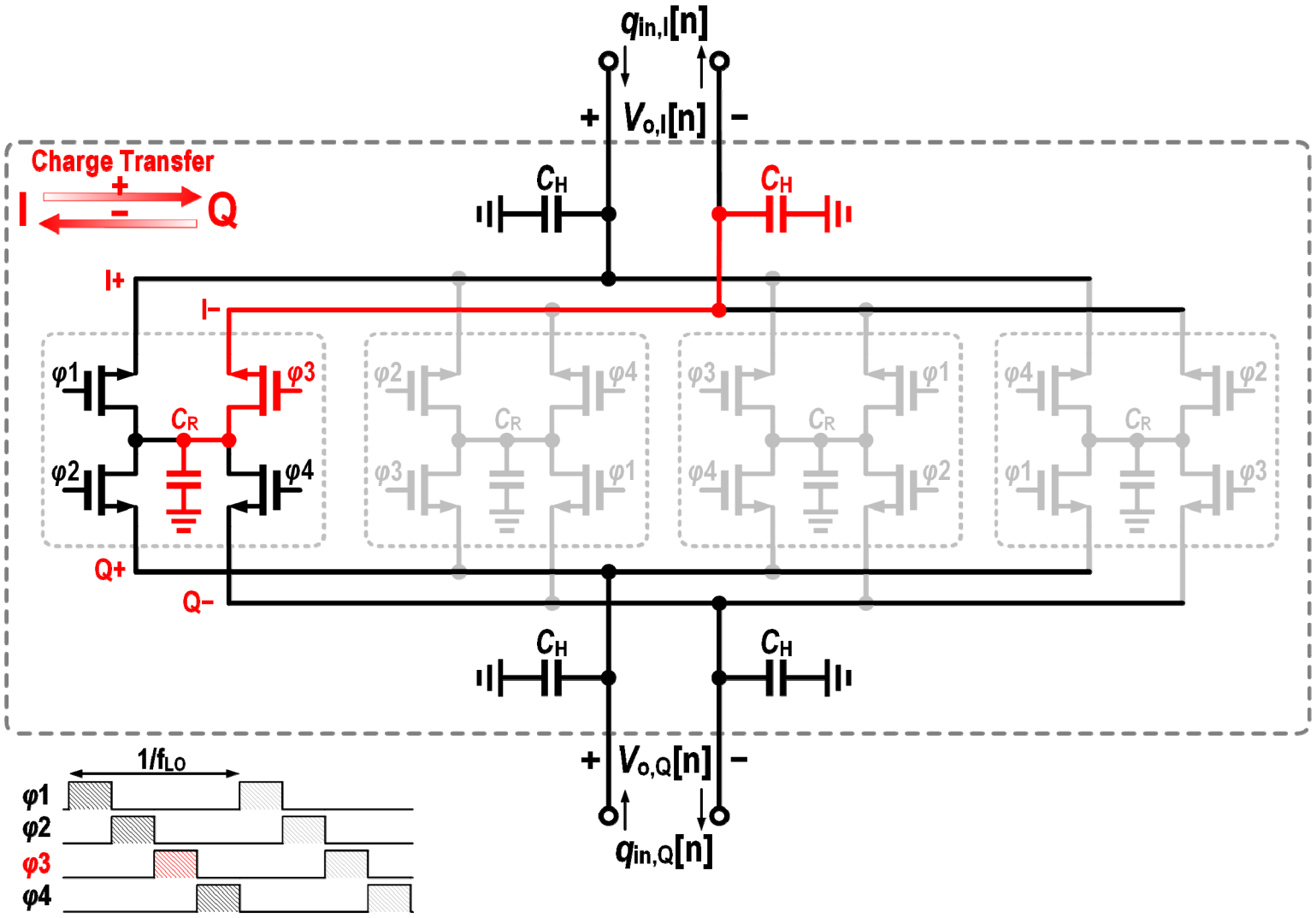
I/Q Charge-Sharing Complex BPF



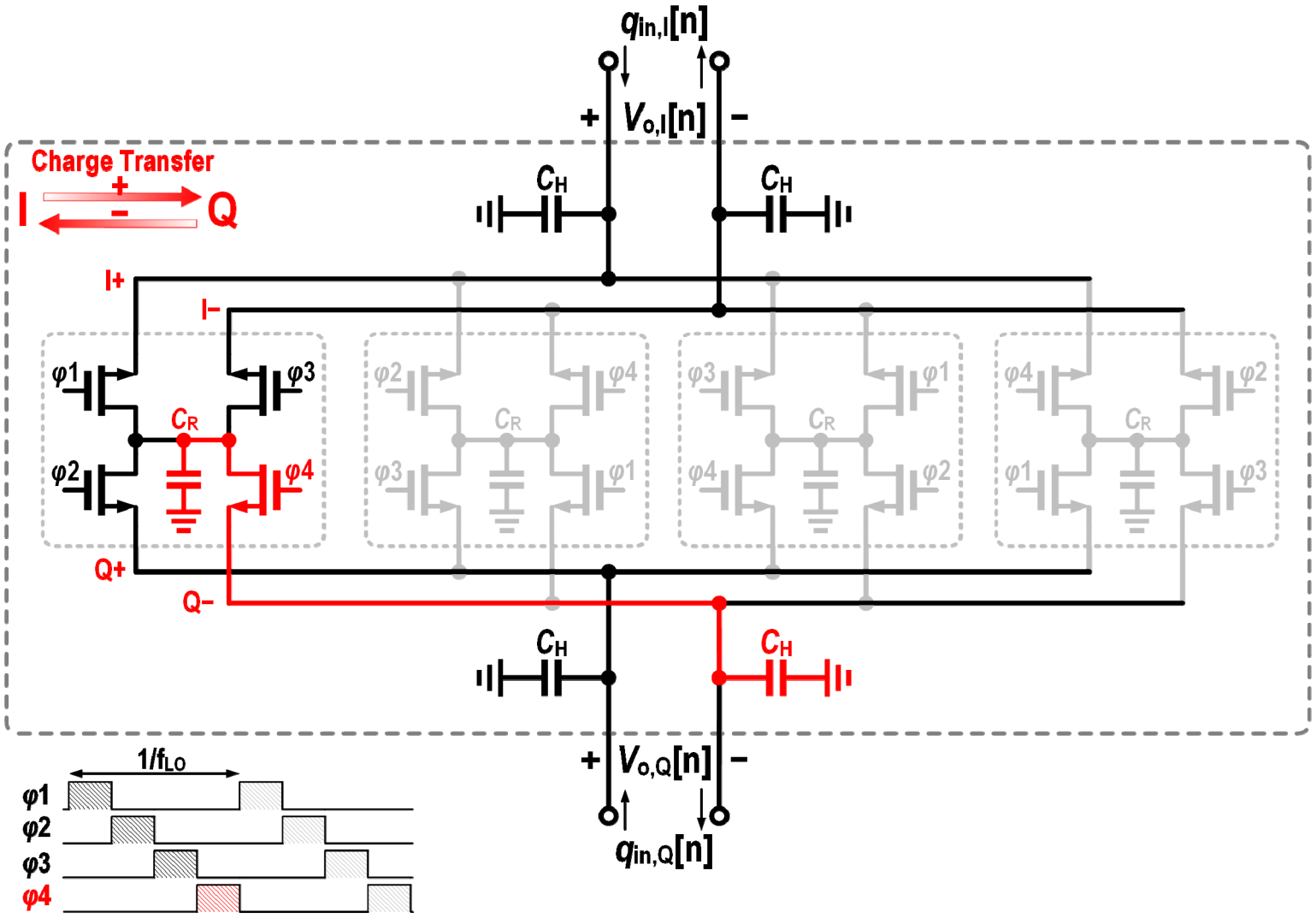
I/Q Charge-Sharing Complex BPF



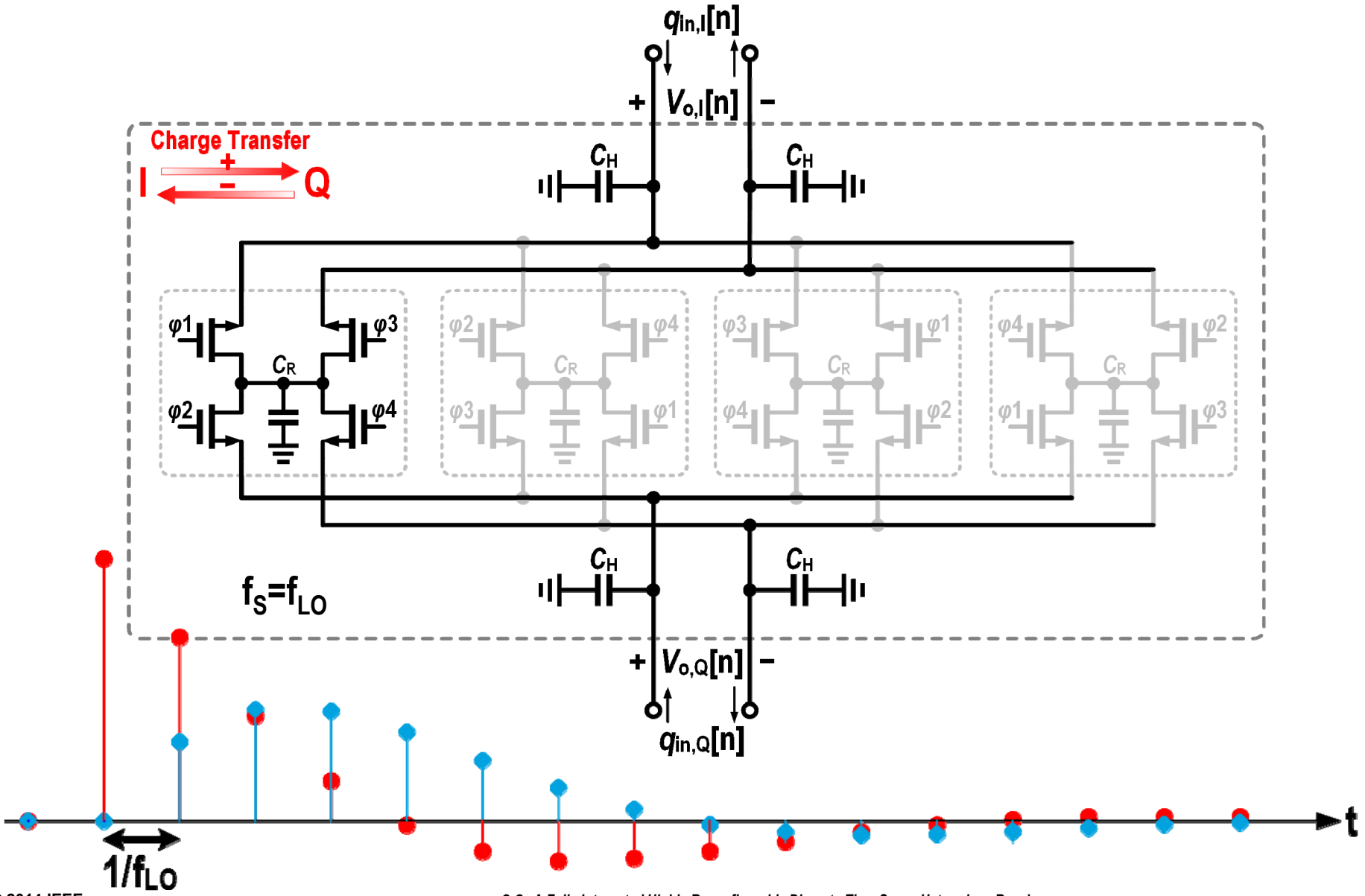
I/Q Charge-Sharing Complex BPF



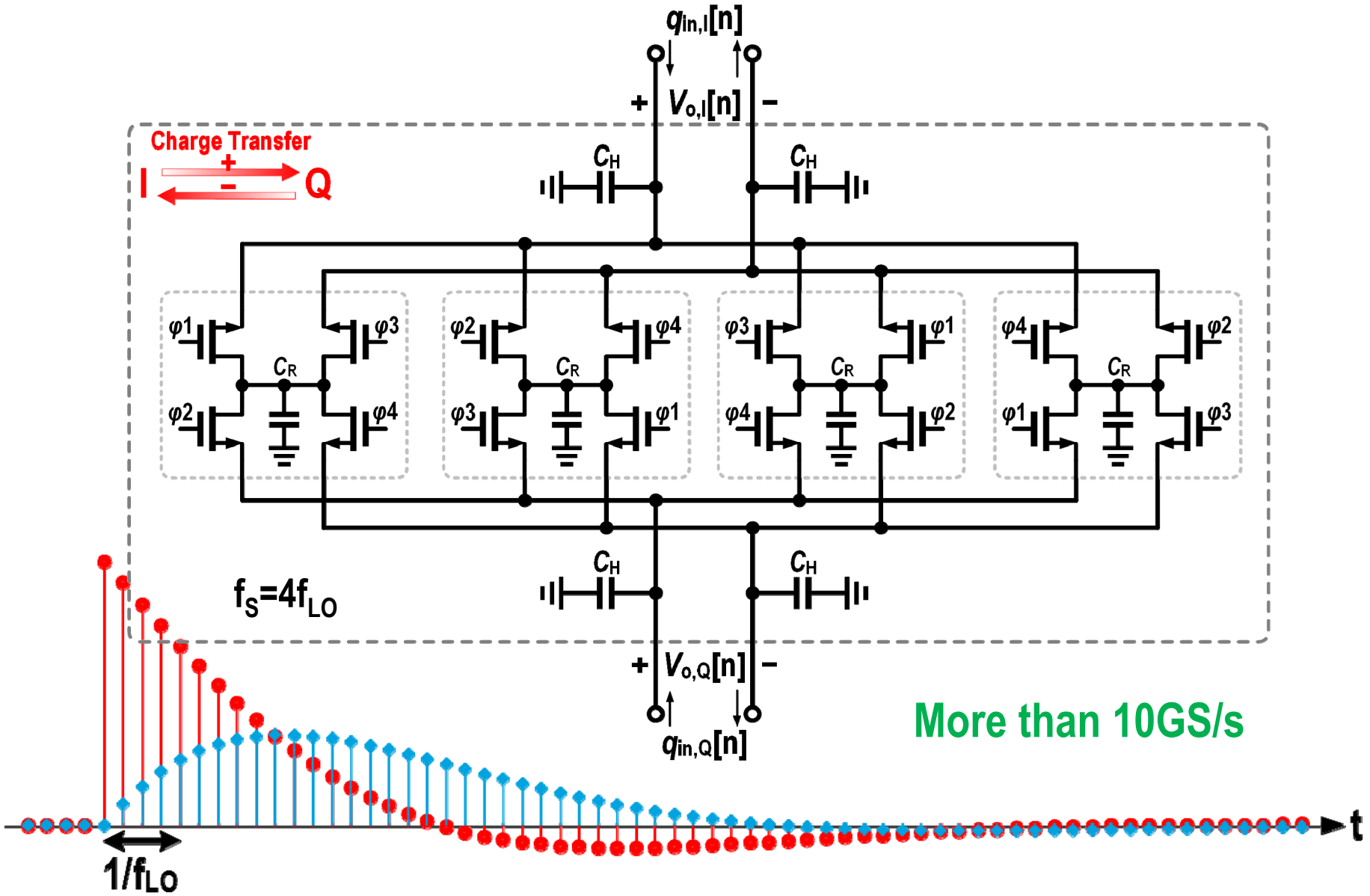
I/Q Charge-Sharing Complex BPF



Impulse Response of CS-BPF (1x rate)



Impulse Response of CS-BPF (4x rate)



Transfer Function of CS-BPF

History on I path

Charge coming from Q to I path

Input charge to I path

$$V_o = V_{o,I} + j \cdot V_{o,Q}$$

$$\begin{cases} V_{o,I}[n] = \alpha \cdot V_{o,I}[n-1] - (1-\alpha) \cdot V_{o,Q}[n-1] + \dfrac{1}{C_H + C_R} q_{in,I}[n] \\ V_{o,Q}[n] = \alpha \cdot V_{o,Q}[n-1] + (1-\alpha) \cdot V_{o,I}[n-1] + \dfrac{1}{C_H + C_R} q_{in,Q}[n] \end{cases}$$

$$q_{in} = q_{in,I} + j \cdot q_{in,Q}$$

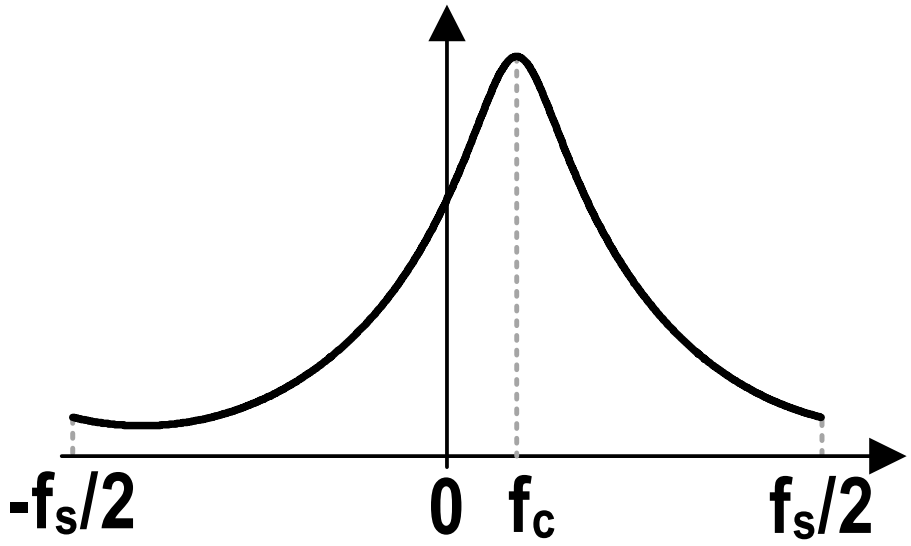
History on Q path

Charge coming from I to Q path

Input charge to Q path

$$\alpha = \frac{C_H}{C_H + C_R}$$

$$1 - \alpha = \frac{C_R}{C_H + C_R}$$

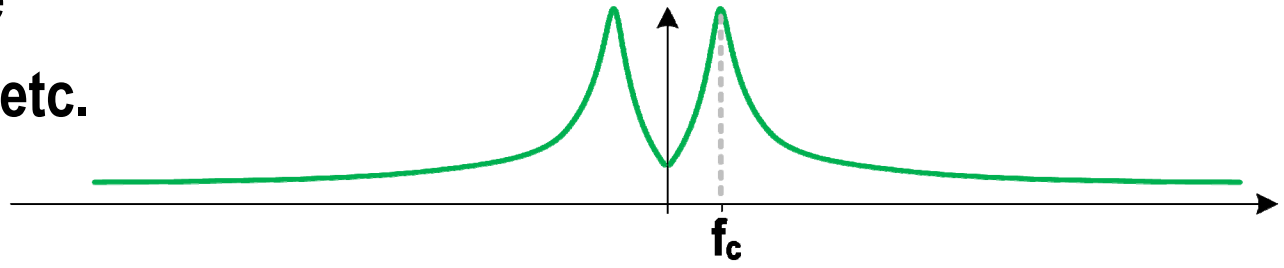


$$H(z) = \frac{V_o}{q_{in}} = \frac{1/(C_H + C_R)}{1 - [\alpha + j(1-\alpha)] z^{-1}}$$

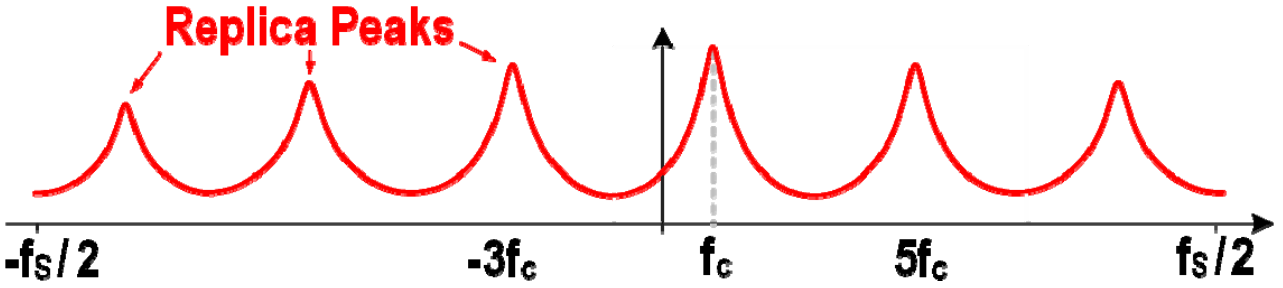
f_c= 50 – 170 MHz

BPF Comparison

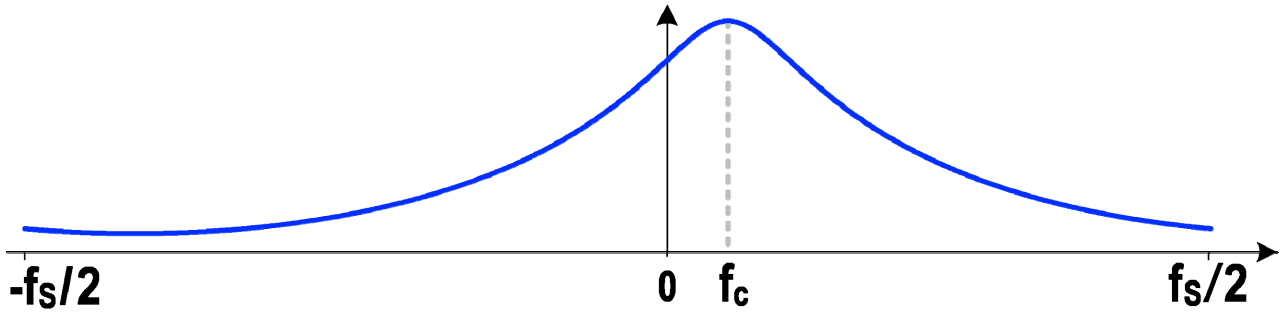
- Continuous-time
  - LC Tank, Gm-C, etc.



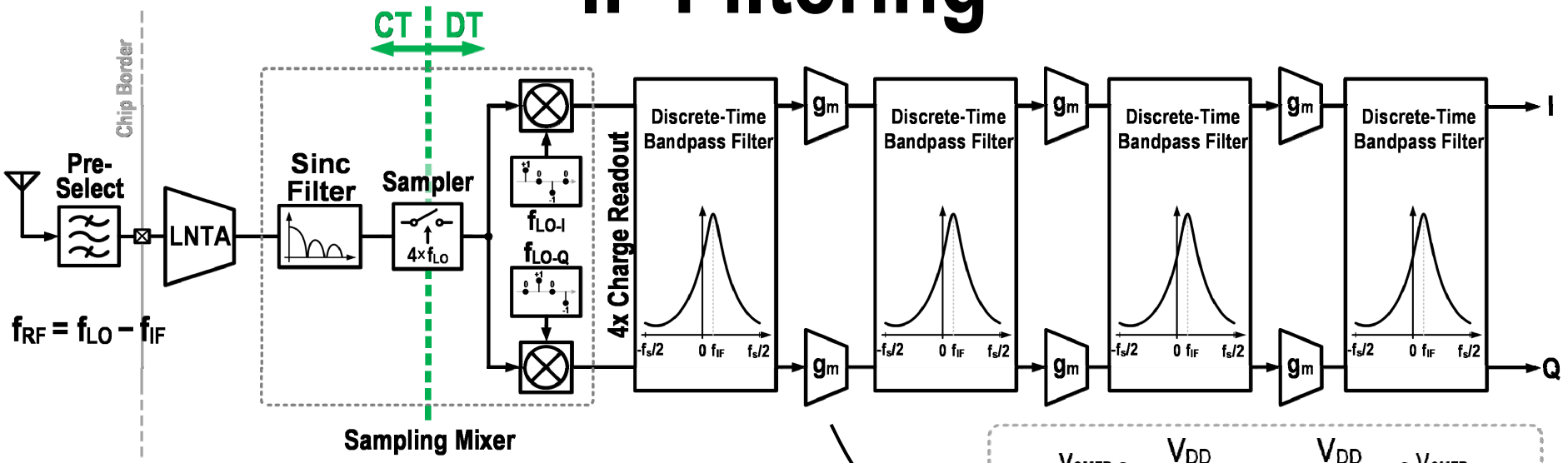
- N-path Filter
  - ✓ High Q
  - ! Replicas
  - ! Limited IIP2

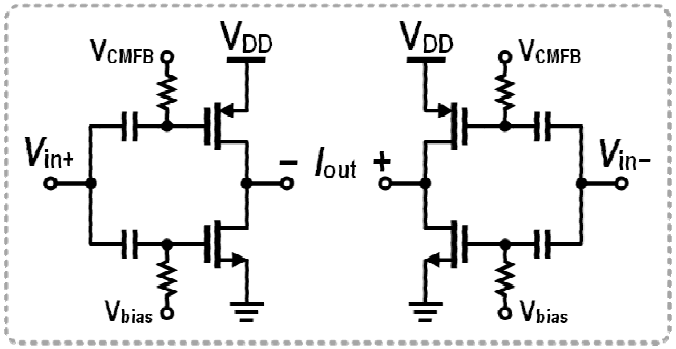


- Complex I/Q Charge-Sharing BPF
  - ✓ No replica
  - ✓ Infinite IIP2
  - ! Lower Q

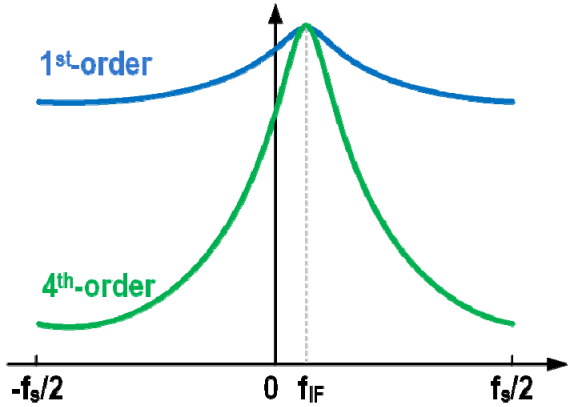


IF Filtering

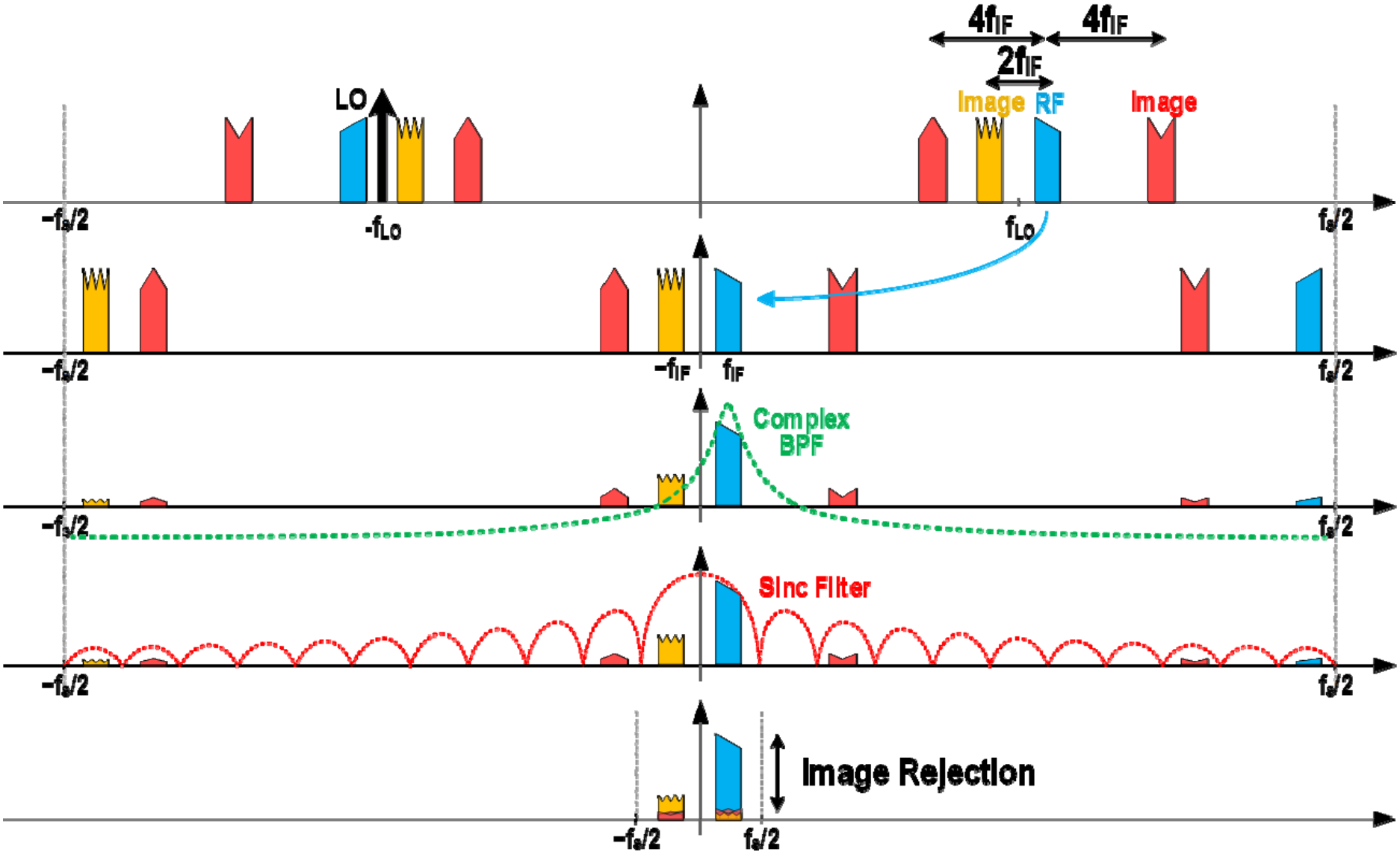




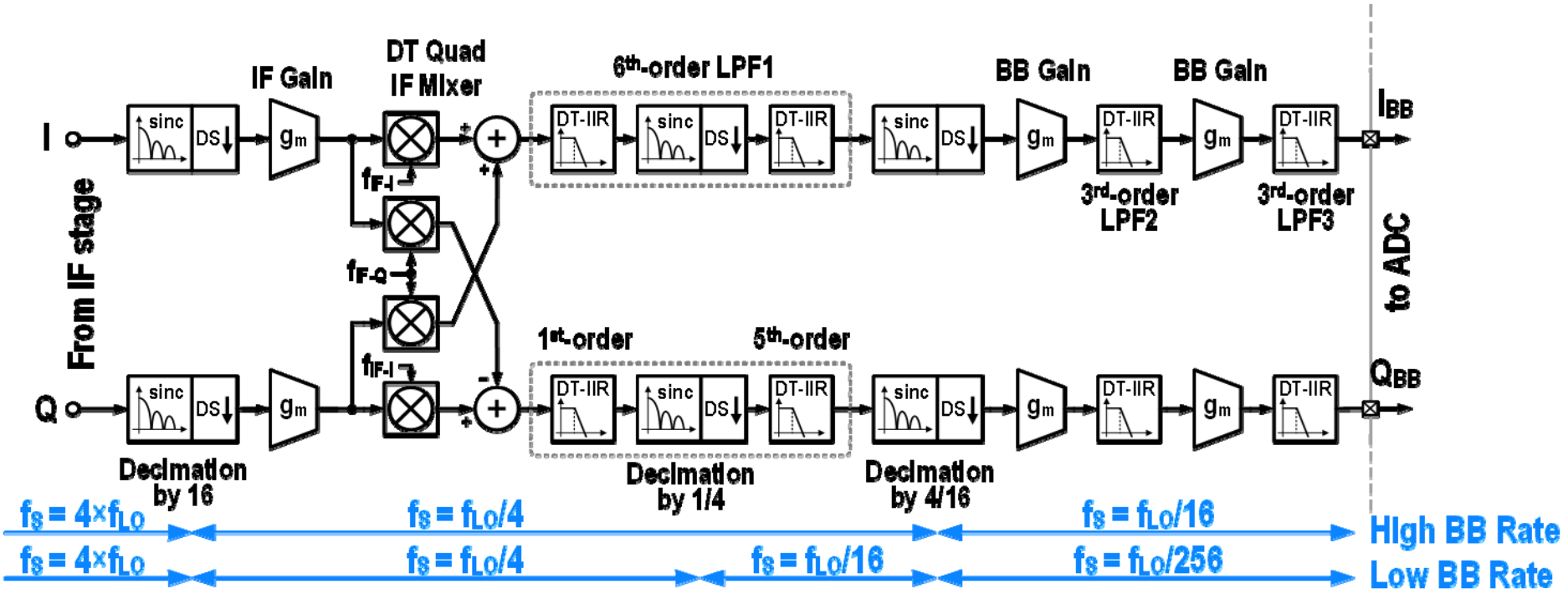
- Increasing order of BPF
  - Filtering blockers
  - Increasing IP3 of following stages
- Keeping 4x rate in all IF filters
- Flicker noise free gain



Frequency Translation

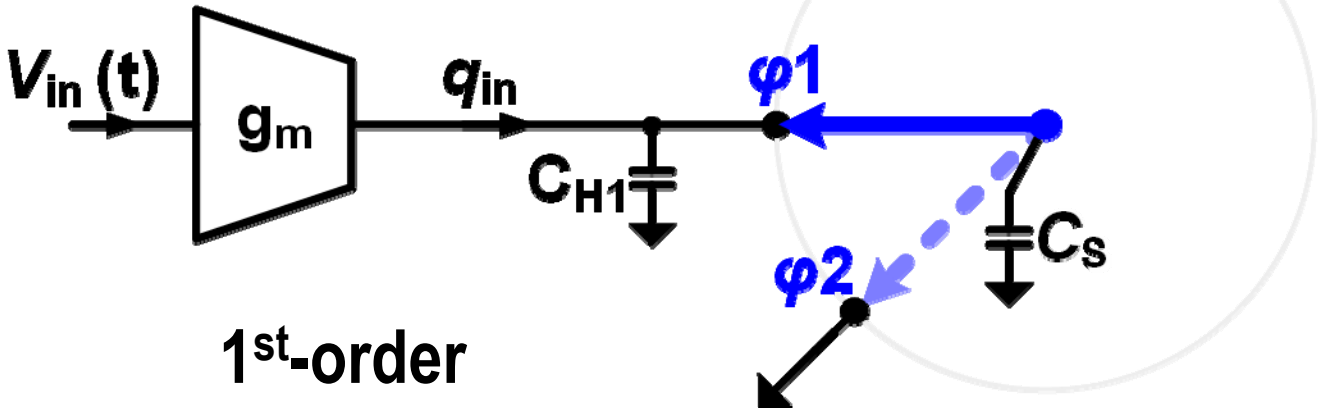


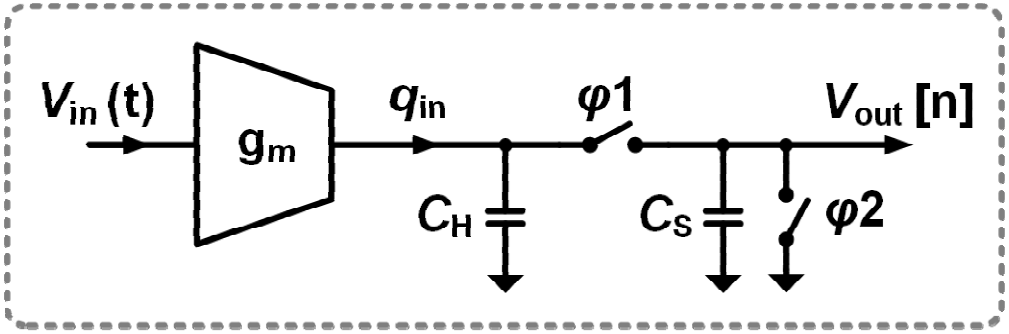
Baseband Signal Processing



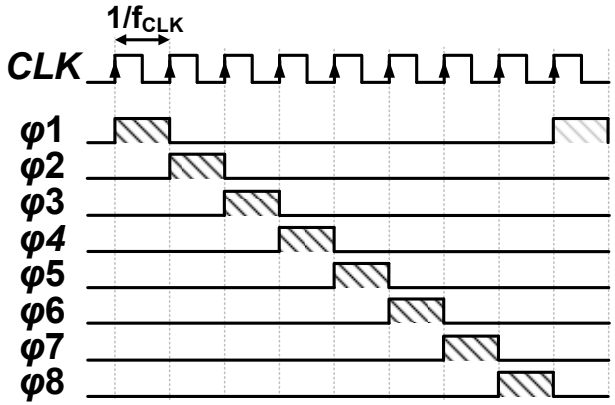
High-Order Low-Pass Filter

- C_H stores the input charge
- φ_1: charge sharing
- φ_2: readout / reset

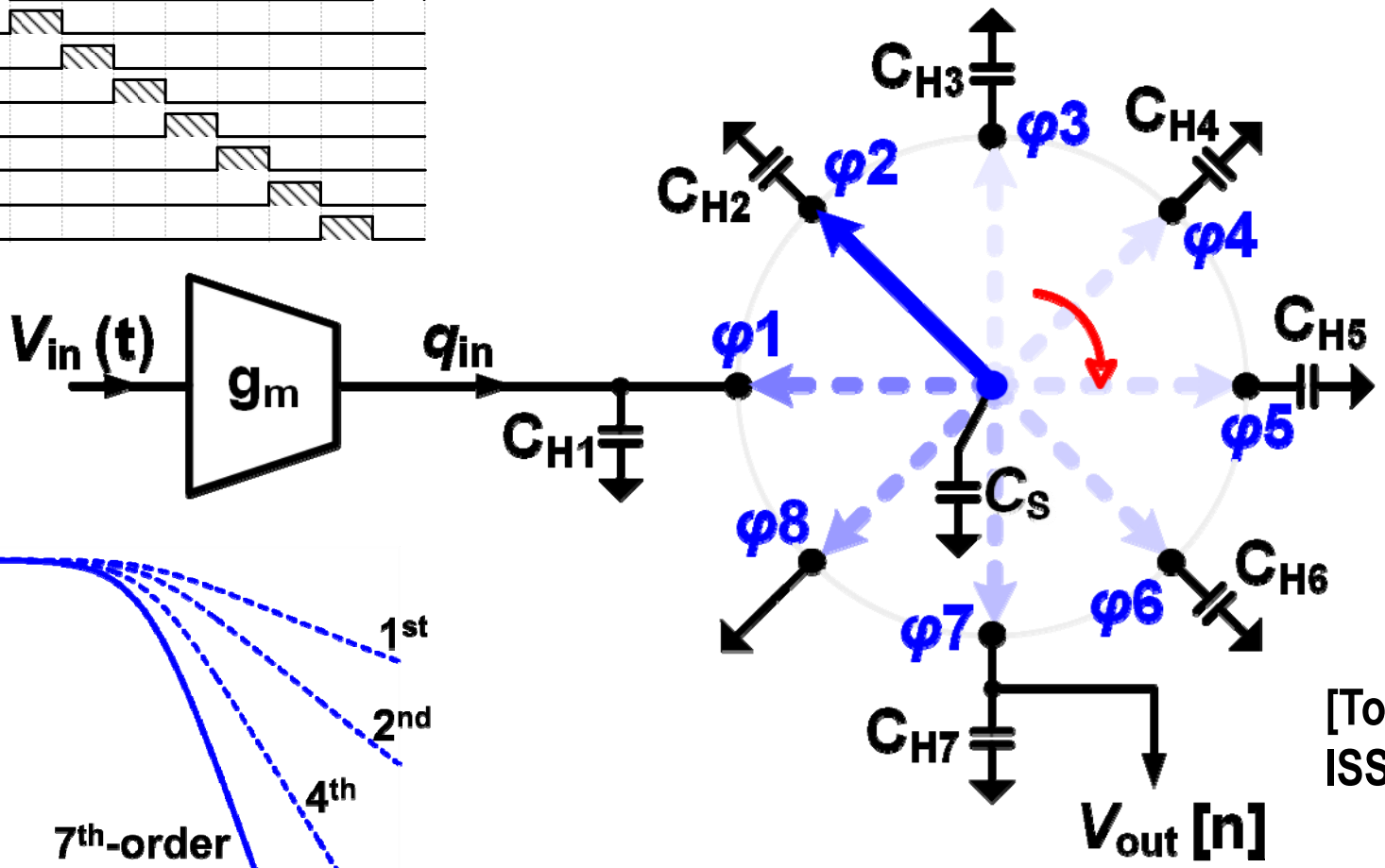




High-Order Low-Pass Filter



7th-order example

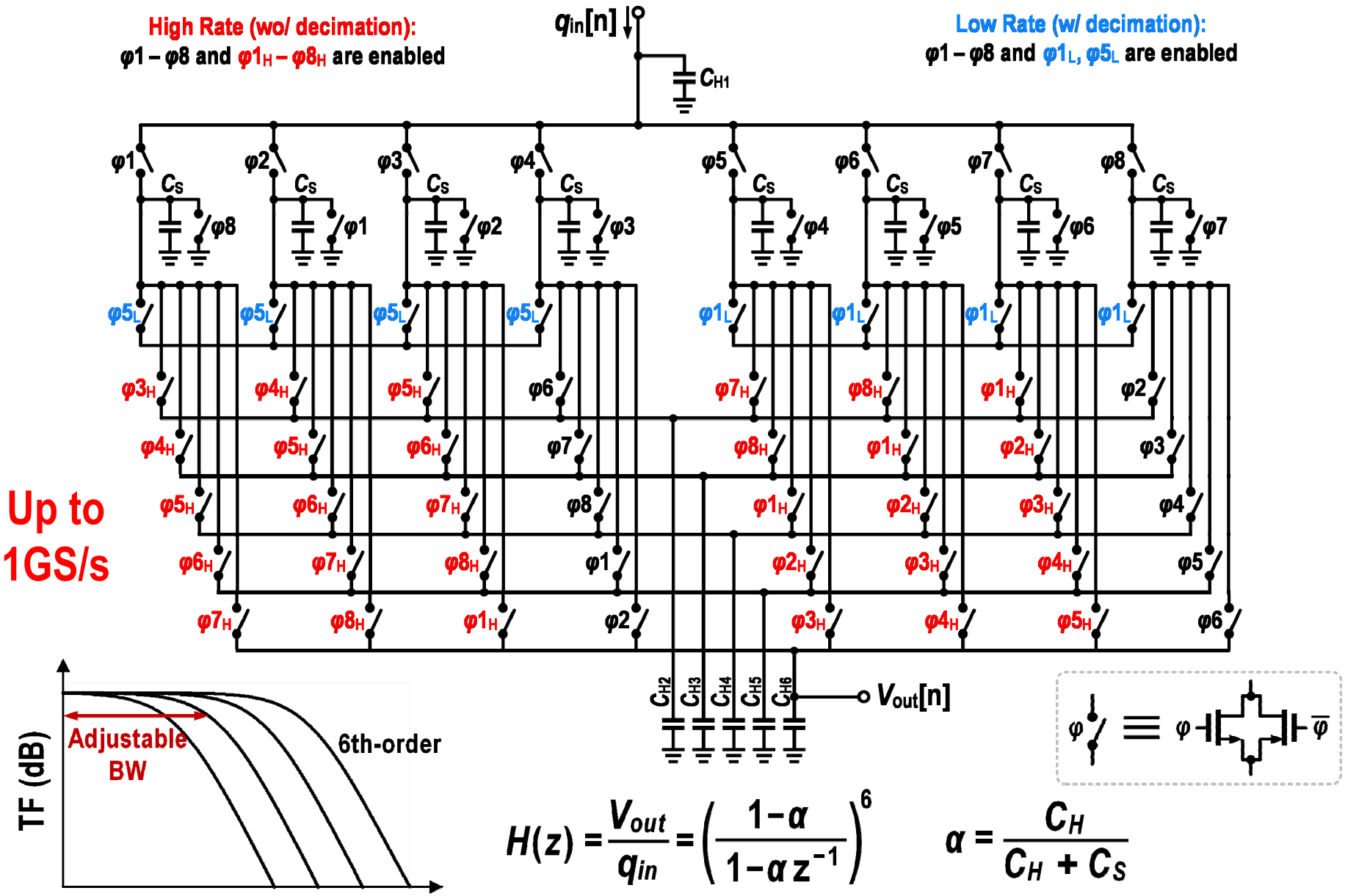


[Tohidian ISSCC'13]

Very low noise: 3nV/√Hz

Highly linear: +15dBm IIP3

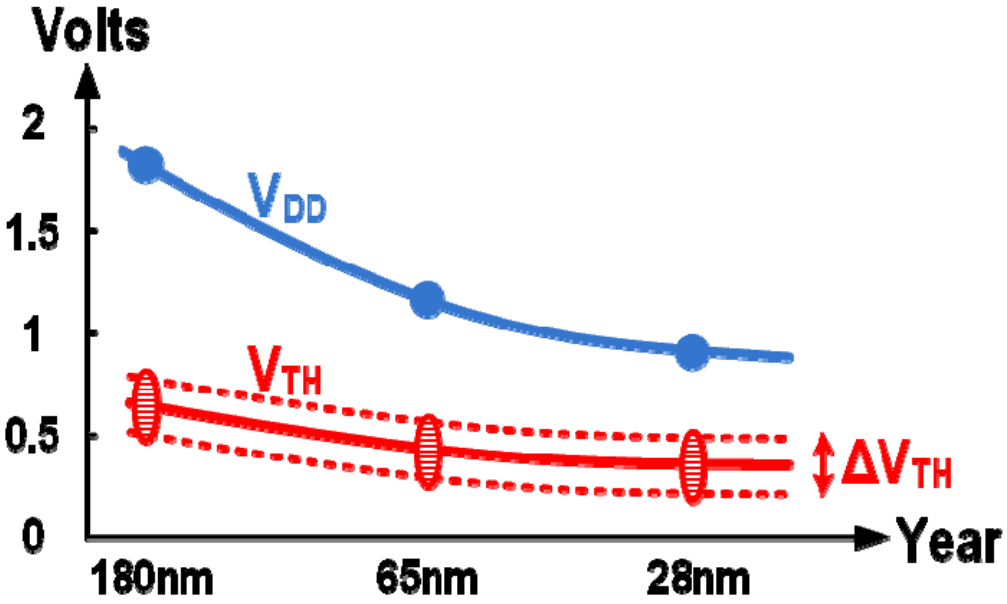
Baseband 6th-order LPF

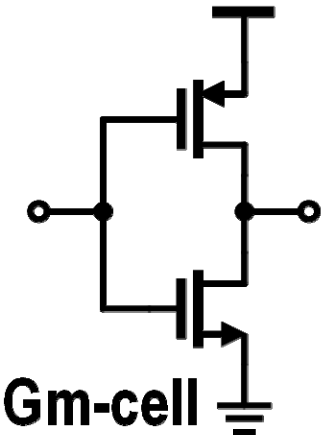


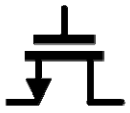
$$H(z) = \frac{V_{out}}{q_{in}} = \left(\frac{1-\alpha}{1-\alpha z^{-1}}\right)^6 \qquad \alpha = \frac{C_H}{C_H + C_S}$$

Why Discrete-Time?

- **Scaling in digital**
  - ✓ Higher speed
  - ✓ Lower power / area
- **Scaling in RF/analog**
  - ✓ Less parasitics
  - ✗ Lower headroom
  - ✗ No power / area scaling
- **Scaling in discrete-time**
  - ✓ Faster digital / switch
  - ✓ Lower power / area
  - ✓ Inverter-based gm





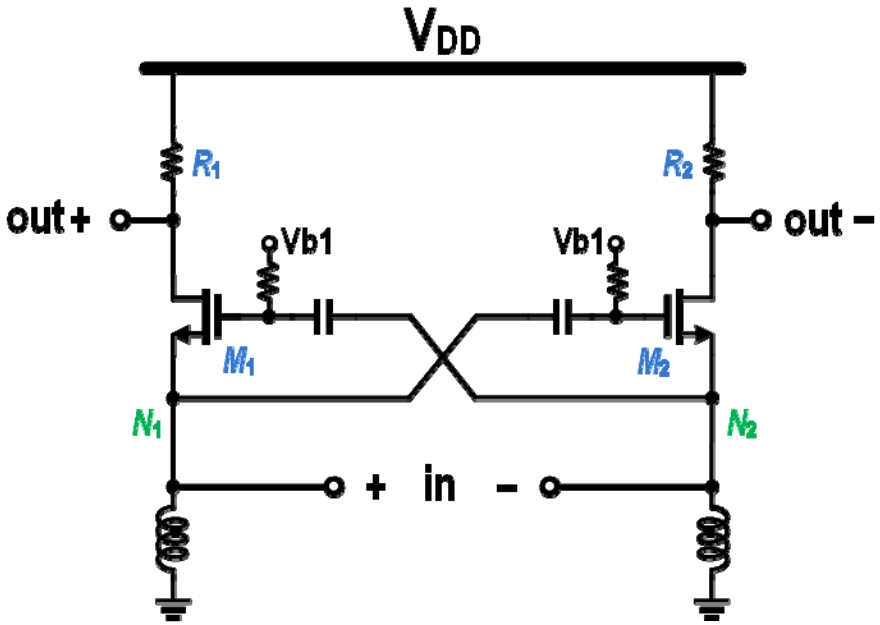


Switch

Capacitor

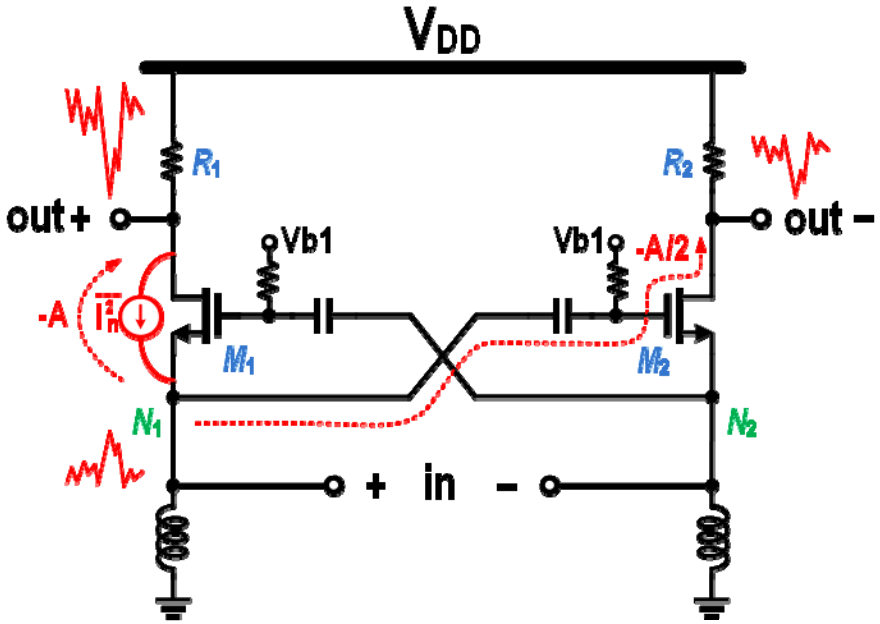
Digital Waveform Generator

Wideband Noise Cancelling LNTA (1)



Cross-coupled common-gate LNA

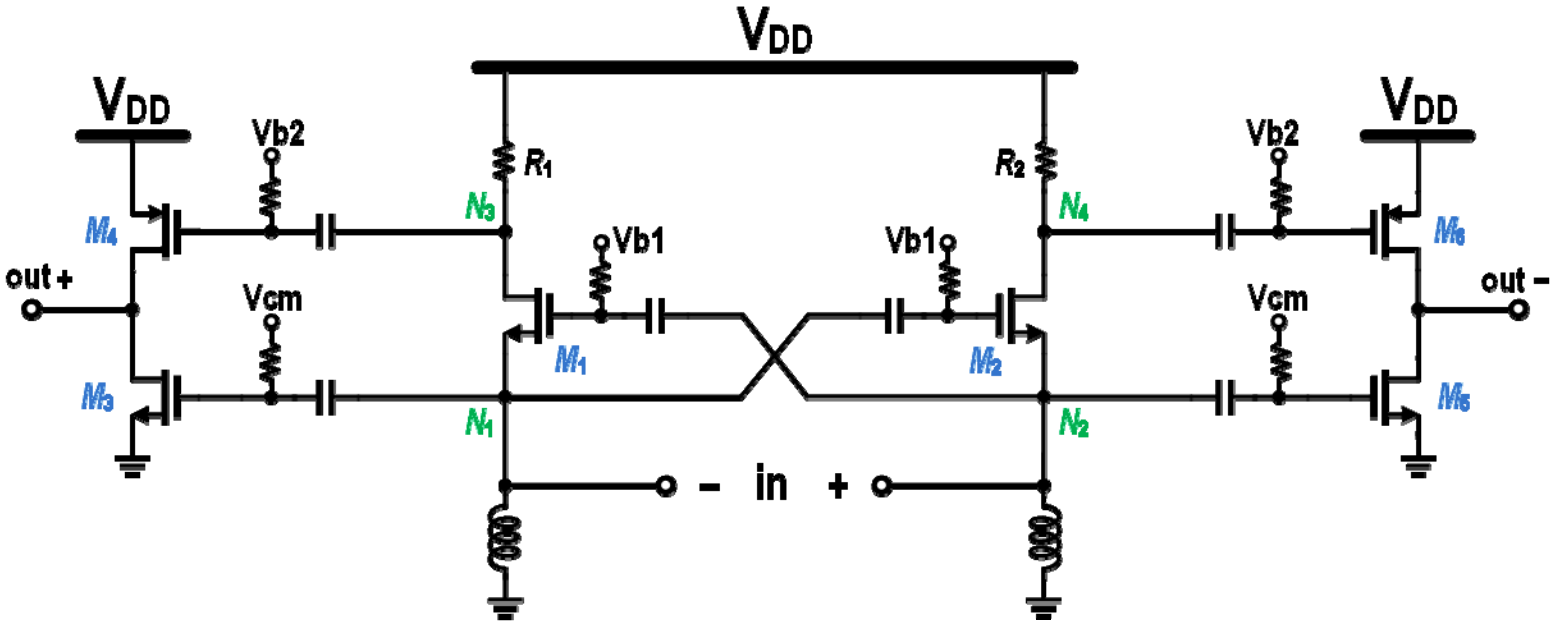
Wideband Noise Cancelling LNTA (1)



1/2 of M1 and M2 noise is converted to common-mode

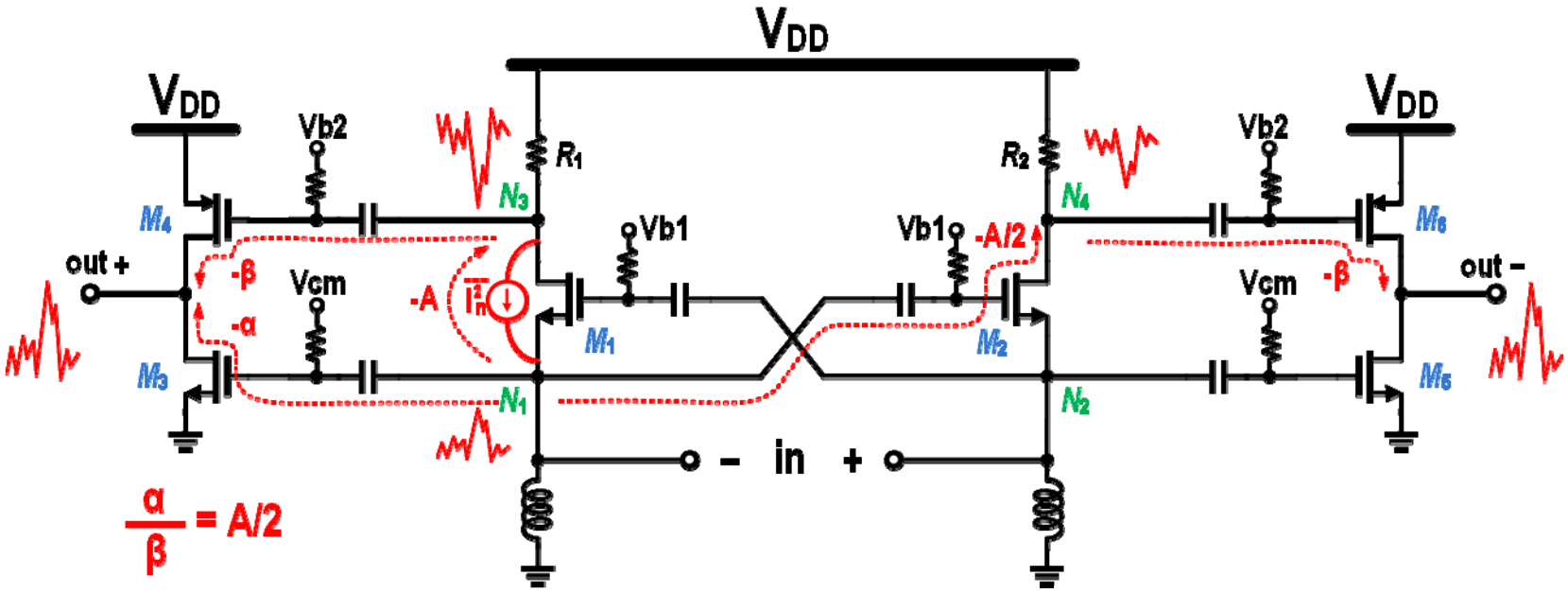
Cross-coupled common-gate LNA

Wideband Noise Cancelling LNTA (2)



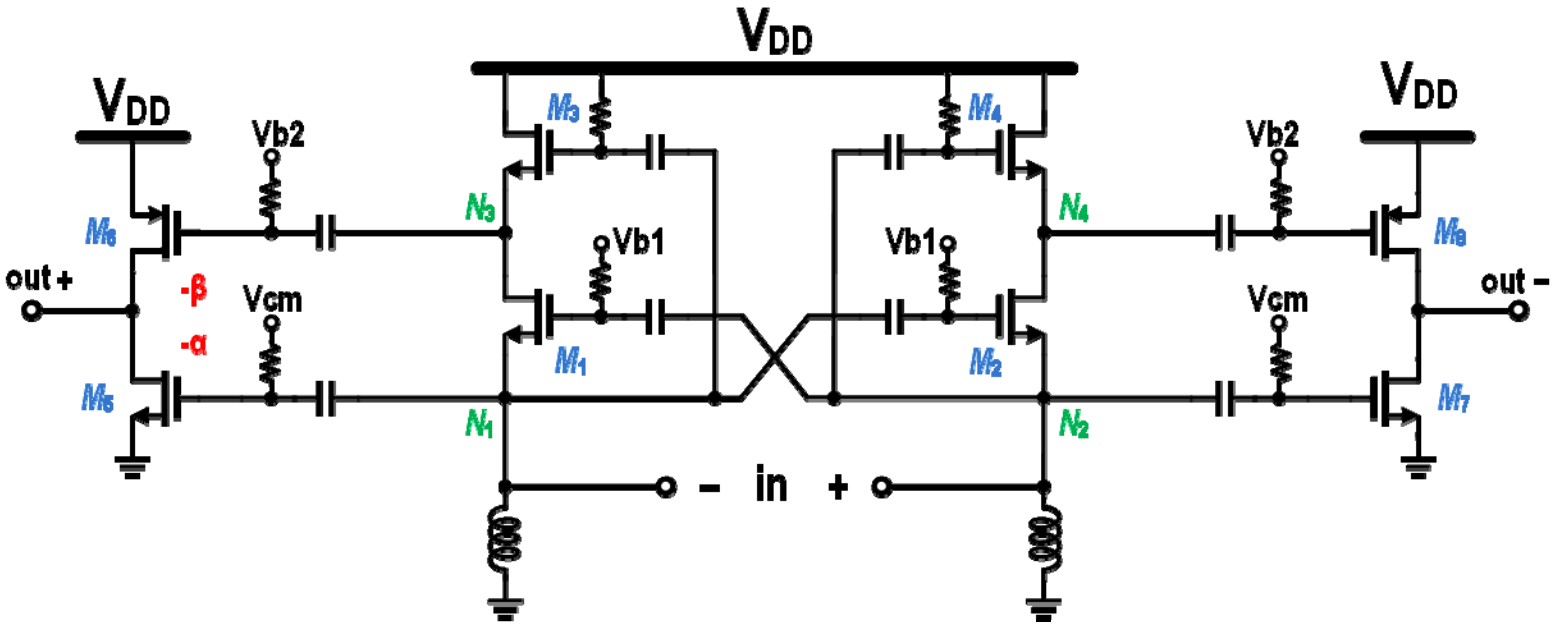
Adding output gm-stage to make LNTA and noise cancelling

Wideband Noise Cancelling LNTA (2)



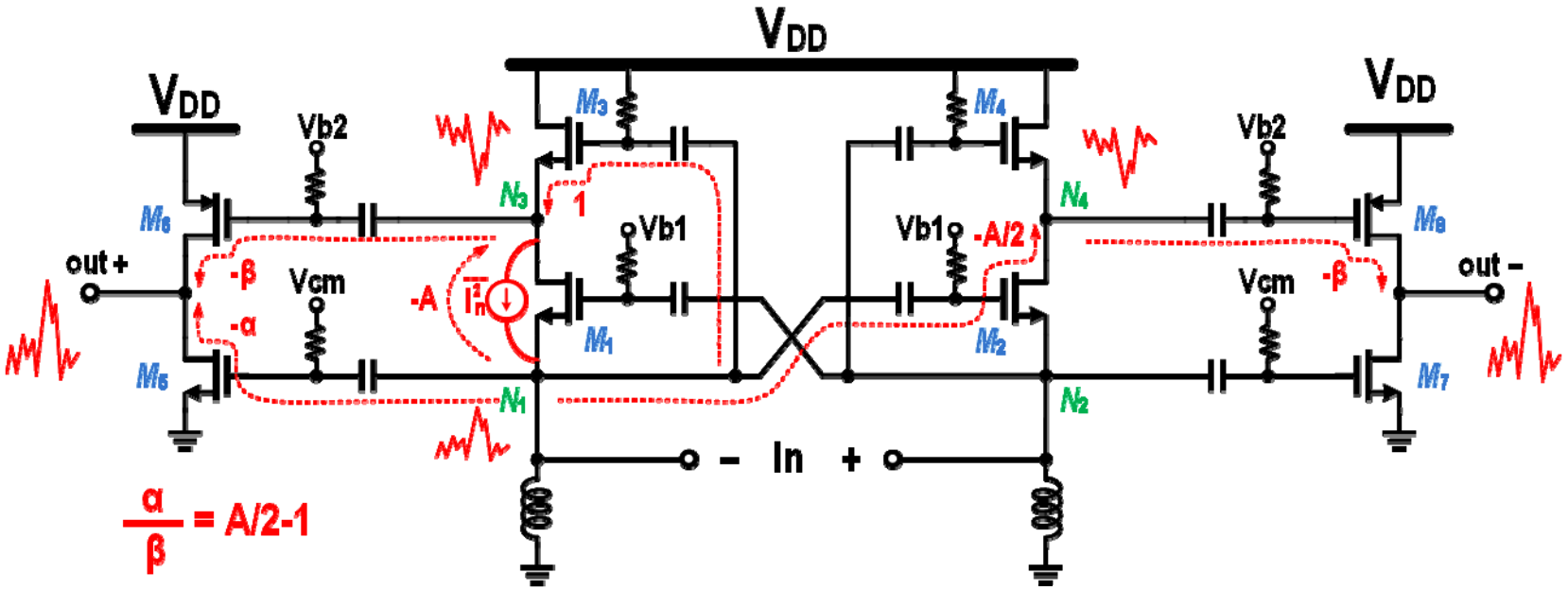
Noise of M1/M2 can be cancelled out completely

Wideband Noise Cancelling LNTA (3)



Replacing resistors with transistors

Wideband Noise Cancelling LNTA (3)

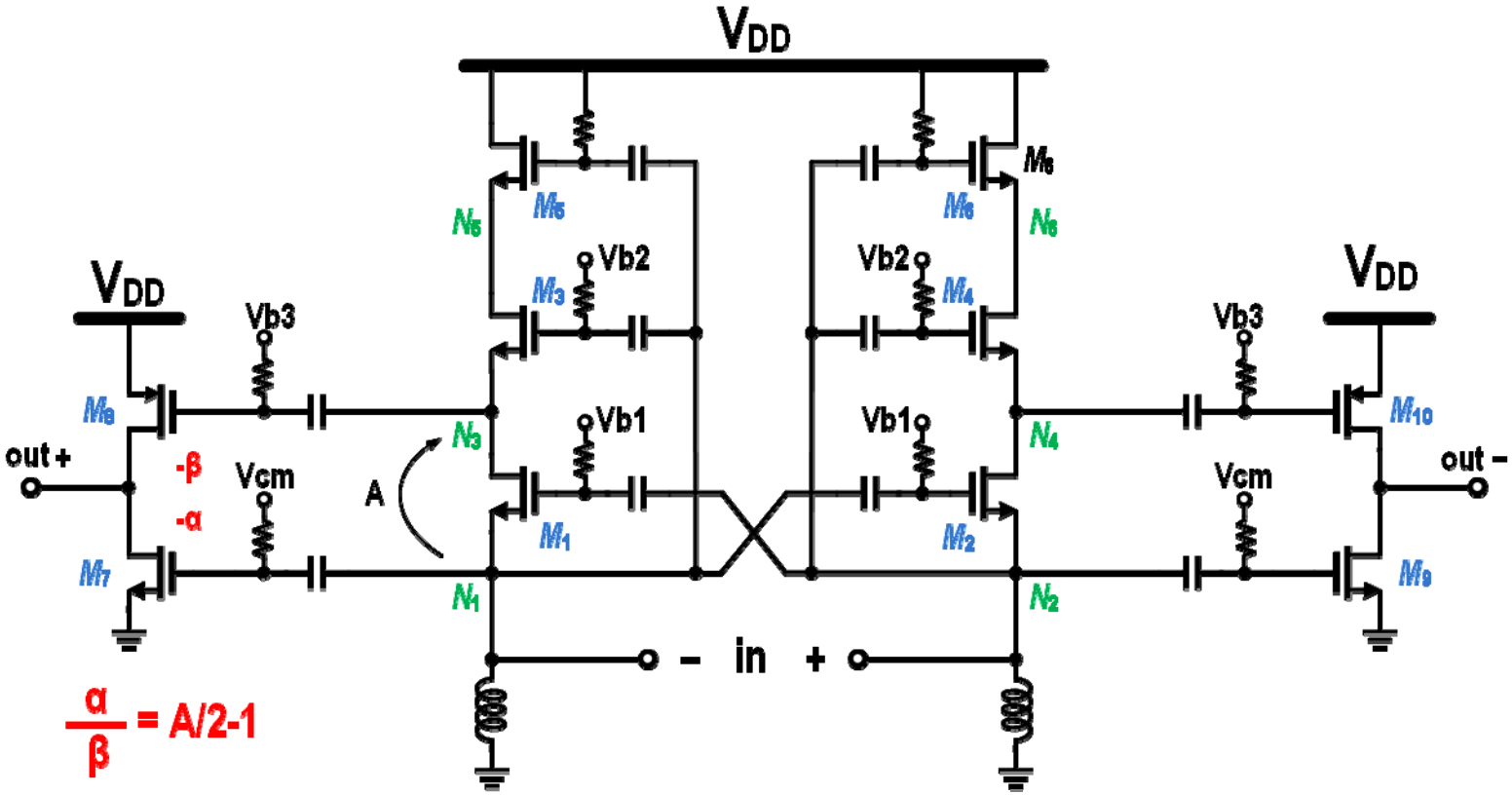


Noise of M1/M2 can be cancelled out completely

A lower α is needed

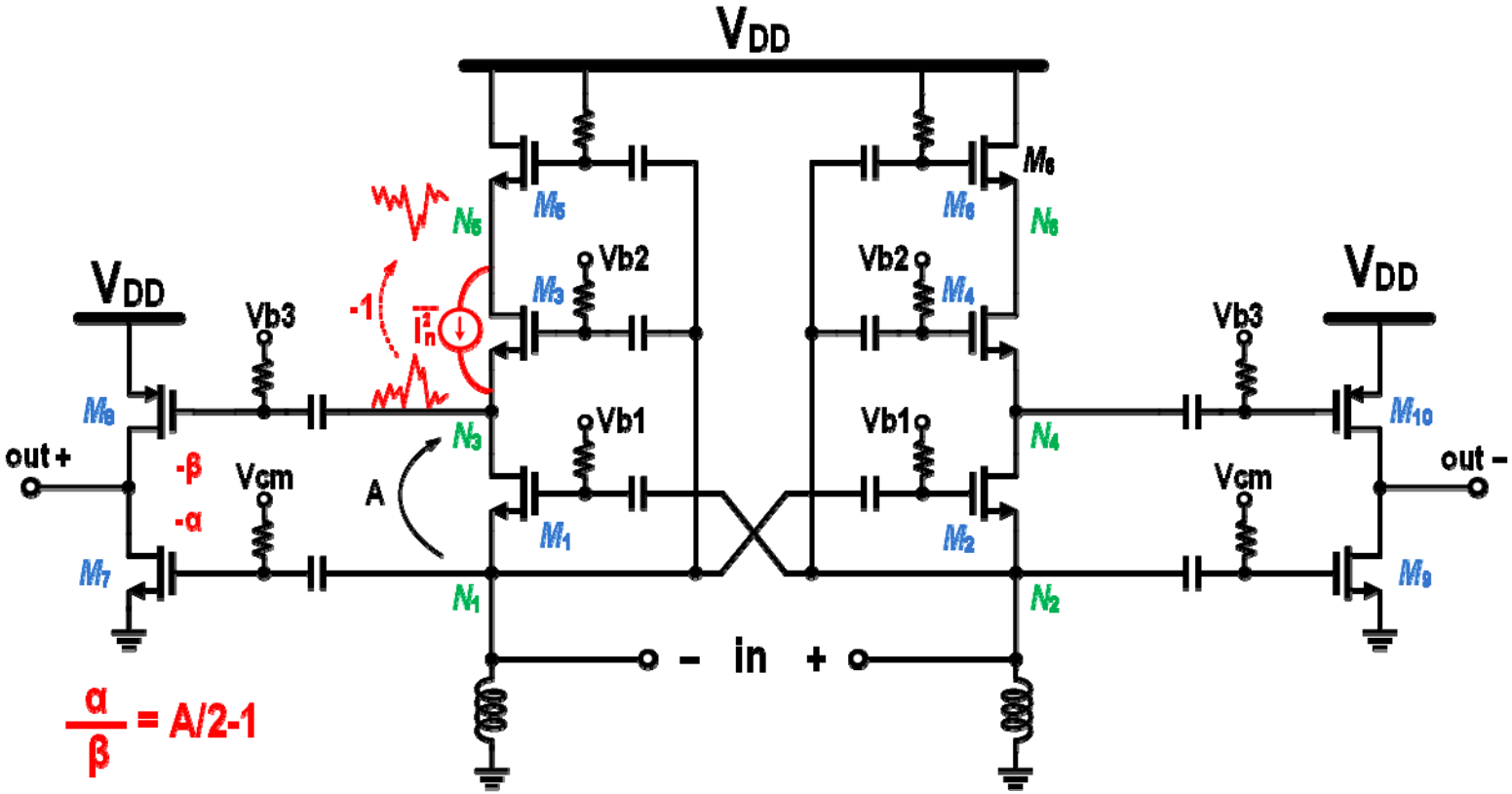
Noise of M3 and M4 still goes to output

Wideband Noise Cancelling LNTA (4)



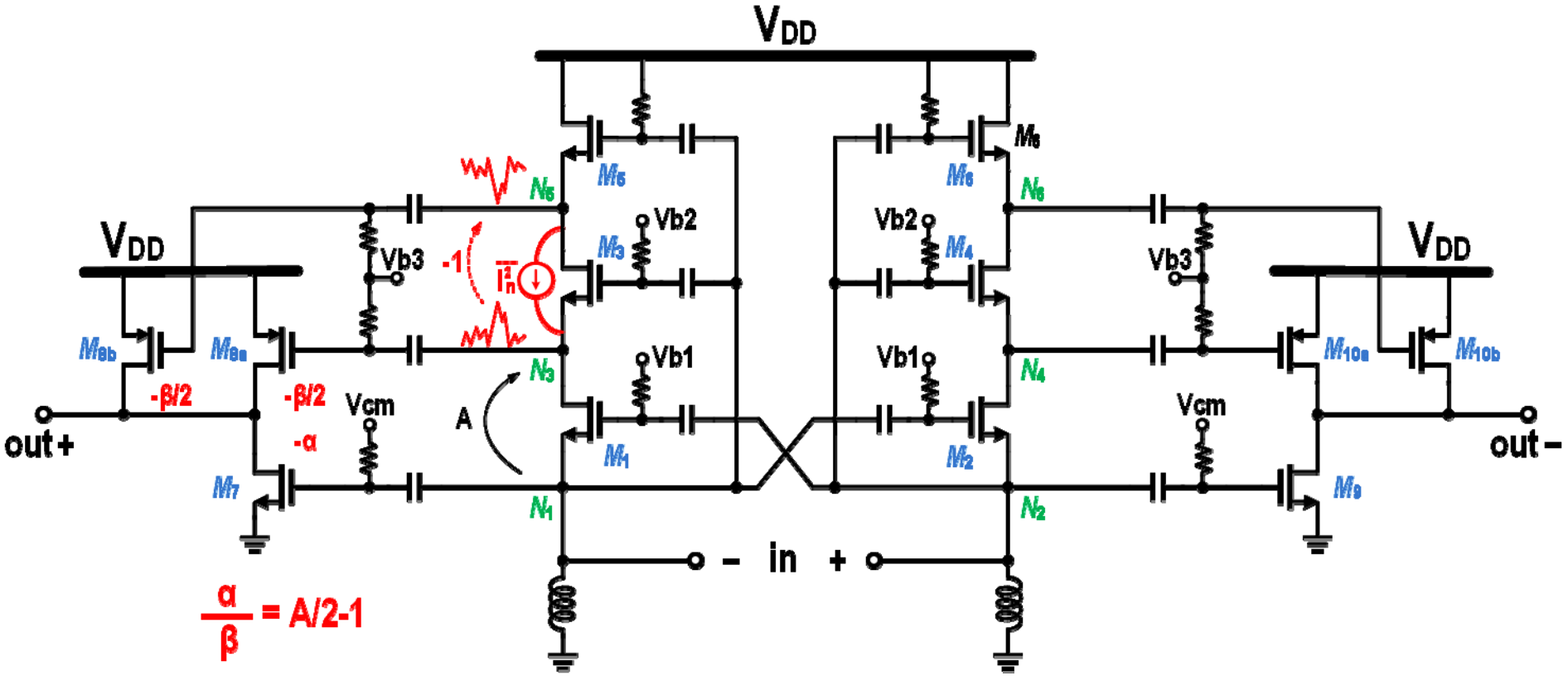
Stacking two more transistors
Nothing is changed yet

Wideband Noise Cancelling LNTA (4)



Noise of M1 appears anti-phase on N3 and N5

Wideband Noise Cancelling LNTA (5)

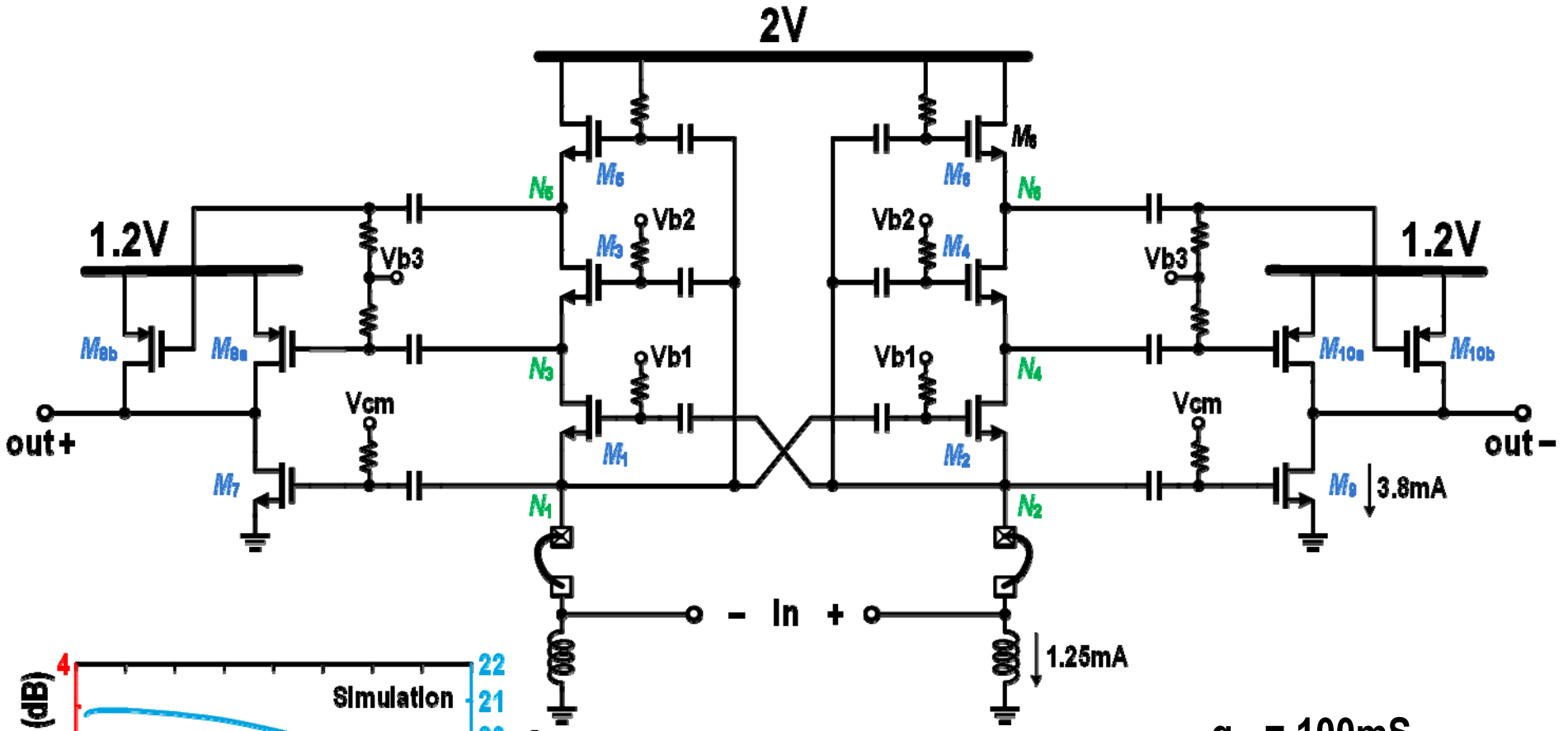


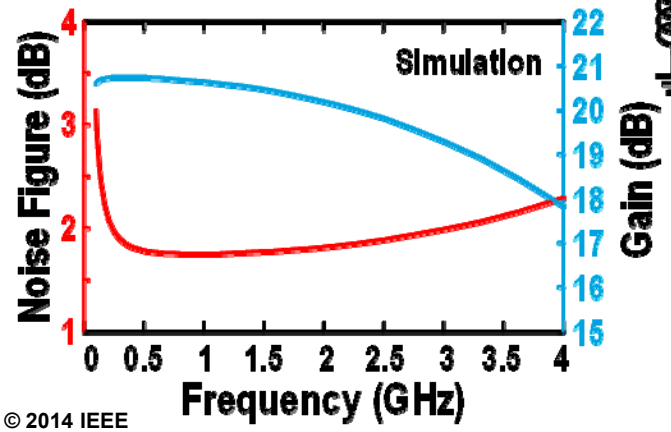
Dividing M8/M10 into two pieces

Noise of M3/M4 is cancelled out

Noise of M5/M6 goes to output with half gain

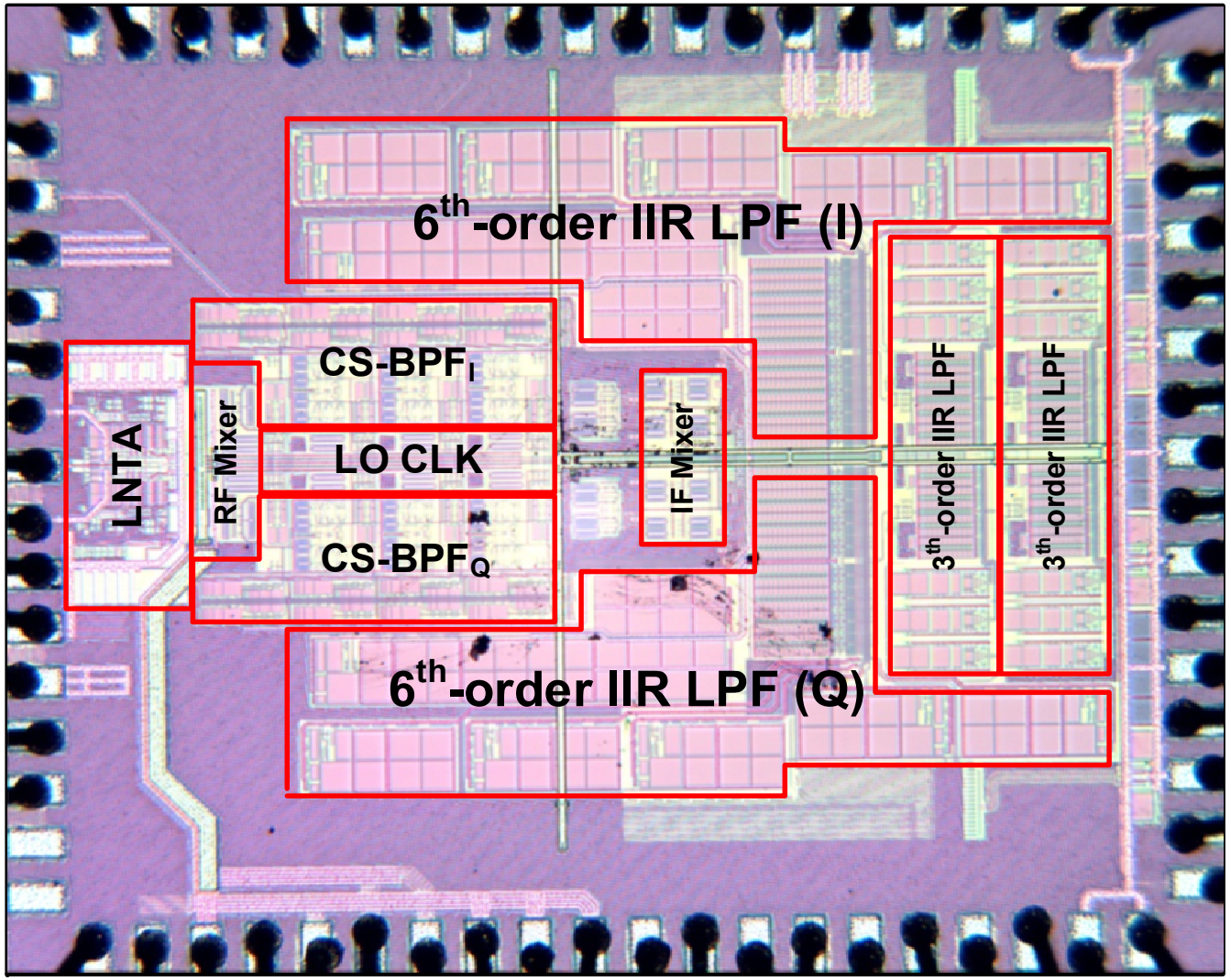
Wideband Noise Cancelling LNTA (5)





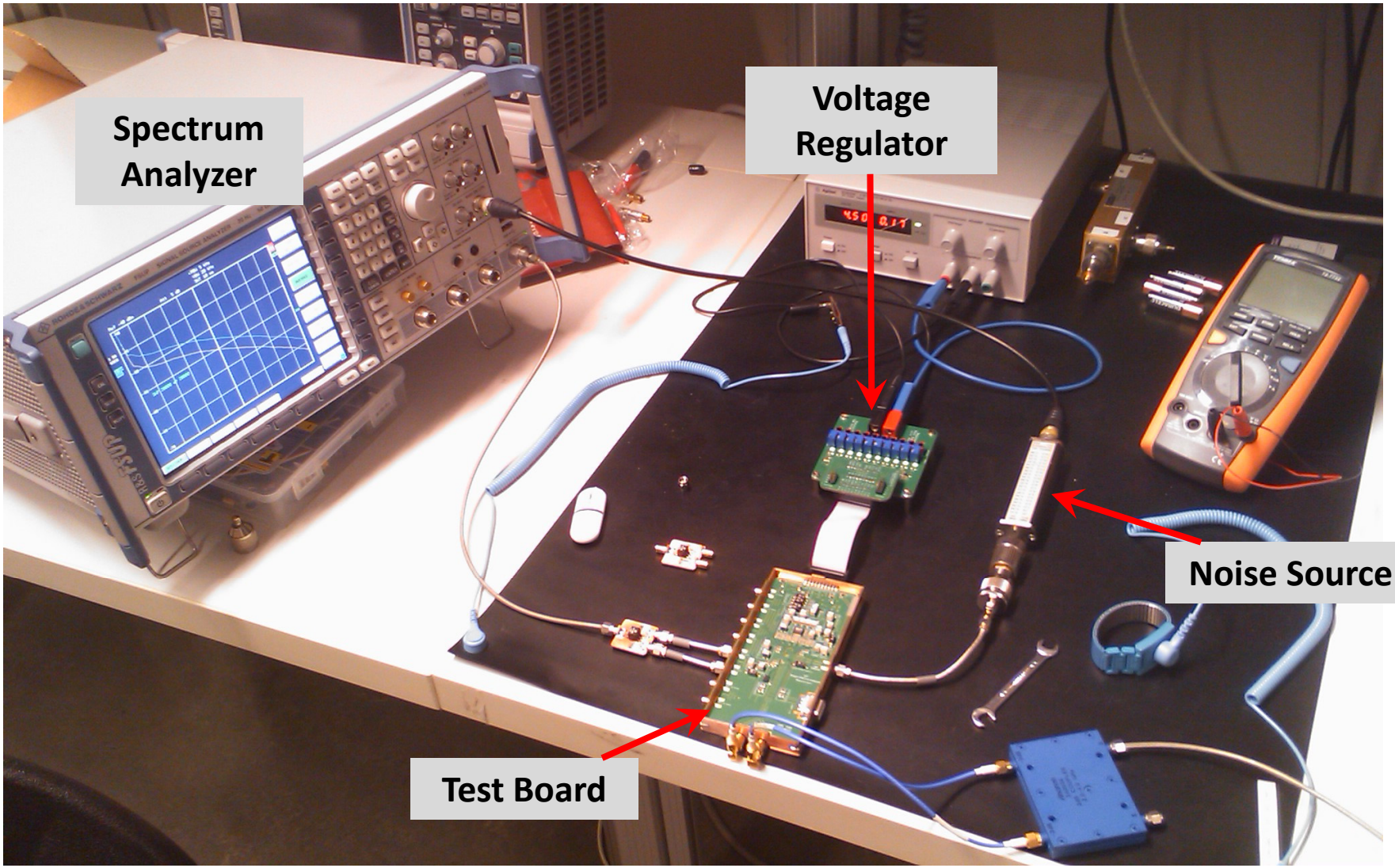
g_m = 100mS
NF_{min} = 1.85dB
IIP3 = 0dBm
P_{tot} = 14mW

Chip Micrograph



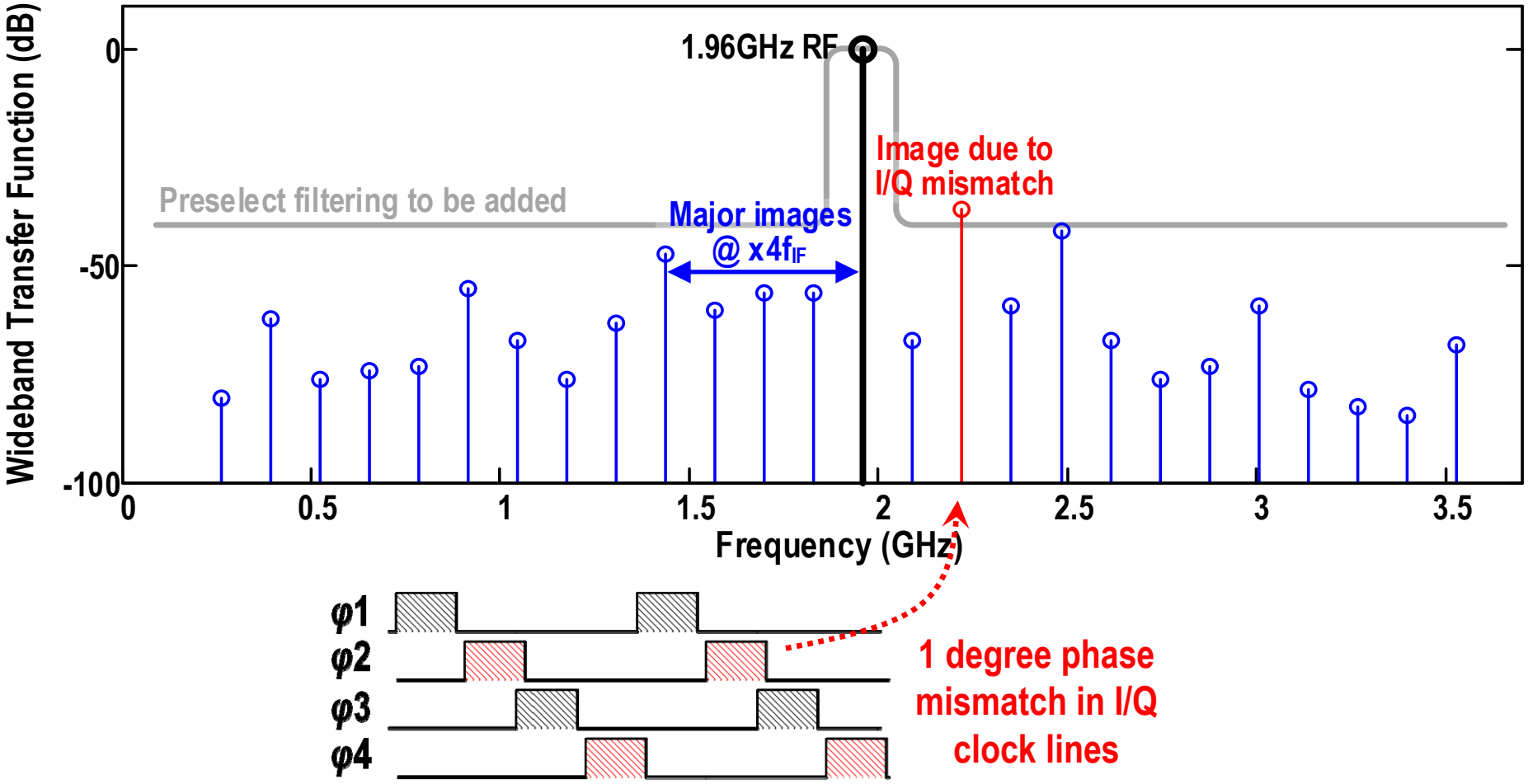
TSMC 65nm CMOS 1.9×2.4mm 1.1mm^2 active

Measurement Setup



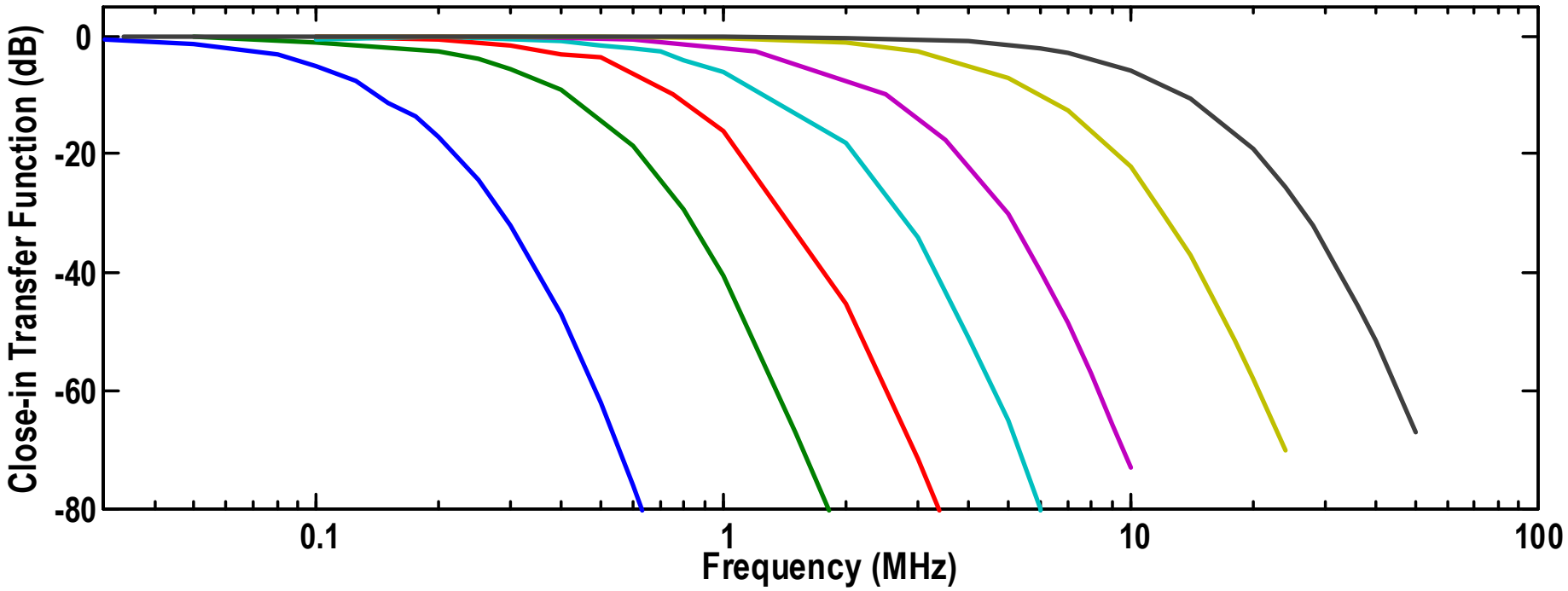
Wideband transfer function

- Major images at $4\times f_{IF}$
- Image rejection > 70dB (including preselect filter)



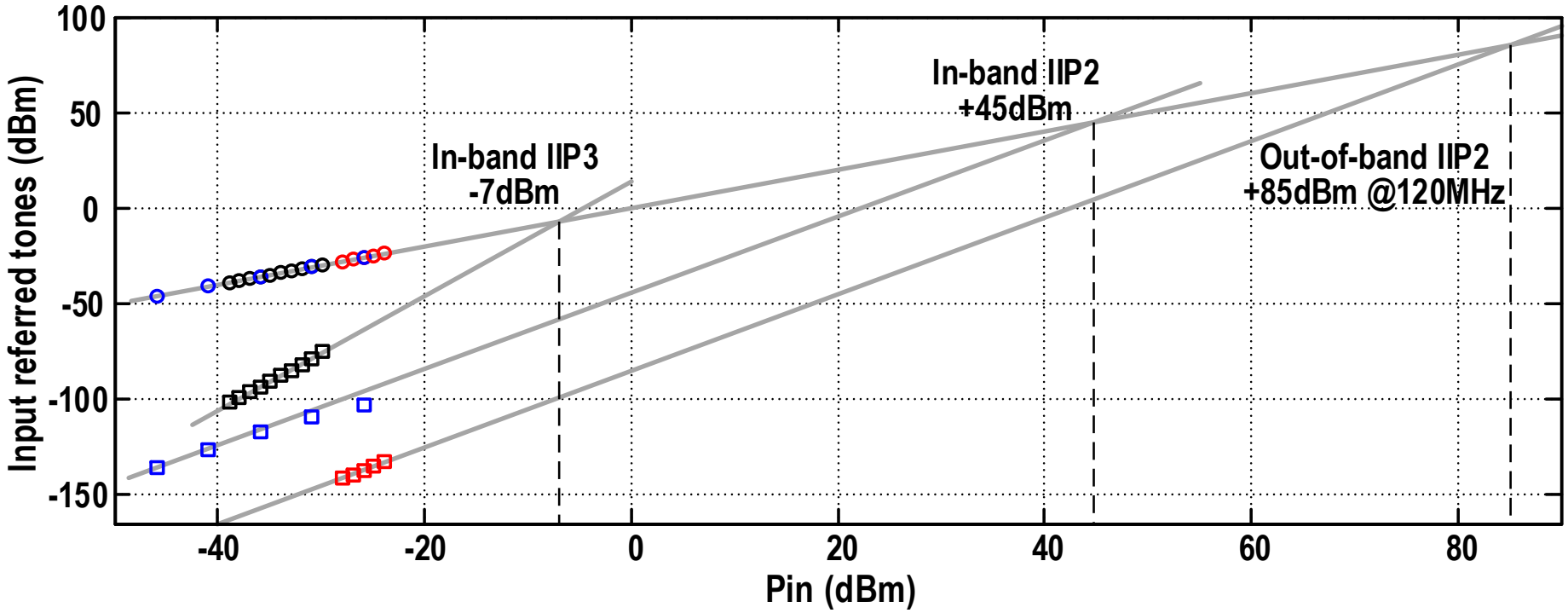
Filtering Transfer Function

- Bandwidth: 200kHz → 20MHz
- 12th-order real poles



Linearity Measurement

- In-band IIP2 limited to IF mixer
  - Improves for far-out frequencies by IF filtering
- IIP3 limited by gm-cell at IF



Comparison with state-of-the-art

	This Work	[Madadi RFIC'13]	[Mirzaei ISSCC'11]	[Geis JSSC'10]
Technology	65nm	65nm	65nm	90nm
Architecture	Superheterodyne	Superheterodyne	Superheterodyne	Homodyne
Analog Baseband	Yes	No	No	Yes
RF Frequency (GHz)	1.8 – 2.5	0.5 – 1.2	1.8 – 2.2	0.5 – 3.8
Supply Voltage (V)	1.2 / 2	1.2	1.2 / 2.5	1.2
Power (mW)	55 – 65	24.5	34	67 – 115
NF (dB)	3.2 – 4.5	7.5	2.8	5.3 – 6.0
Max Gain (dB)	82	35	55	58 / 64
In-band IIP3 (dBm)	-7	+10	-8.5	+1 / +2.5
In-band IIP2 (dBm)	+45 §	–*	–*	–*
Out-of-band IIP2 (dBm)	+85 §	–*	–*	+38 / +52
Channel BW (MHz)	0.2 – 20	4.5	4	0.2 – 20
Area (mm^2)	1.1	0.45	0.76	0.5

* Not reported § Without calibration

Conclusion

- Demonstrated the first-ever full chain of discrete-time superheterodyne receiver
  - Process scalable in advanced CMOS technology
  - 28nm? No problem!
- Full-rate I/Q charge-sharing bandpass filter at IF
  - Proposing 4x sampling concept for high-IF DT receiver
  - Avoiding early decimation of signal before enough filtering
- Achieving:
  - Getting rid of varying DC offset, LO leakage, flicker noise, etc.
  - Very high uncalibrated out-of-band IIP2

Acknowledgement

- I would like to acknowledge my wife Zahra and my colleagues Amir Reza Ahmadimehr, Morteza Avali, Masoud Babaie and Wanghua Wu.
- We would like to acknowledge Atef Akhnoukh, Wil Straver and Ali Kaichouhi for their help on measurement and assembly.
- We also acknowledge support of HiSilicon.

An RF-to-BB-Current-Reuse Wideband Receiver with Parallel N-Path Active/Passive Mixers and a Single-MOS Pole-Zero LPF

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1 – State-Key Laboratory of Analog and Mixed-Signal VLSI

University of Macau, Macao SAR, China

2 – UMTEC, Macao, China

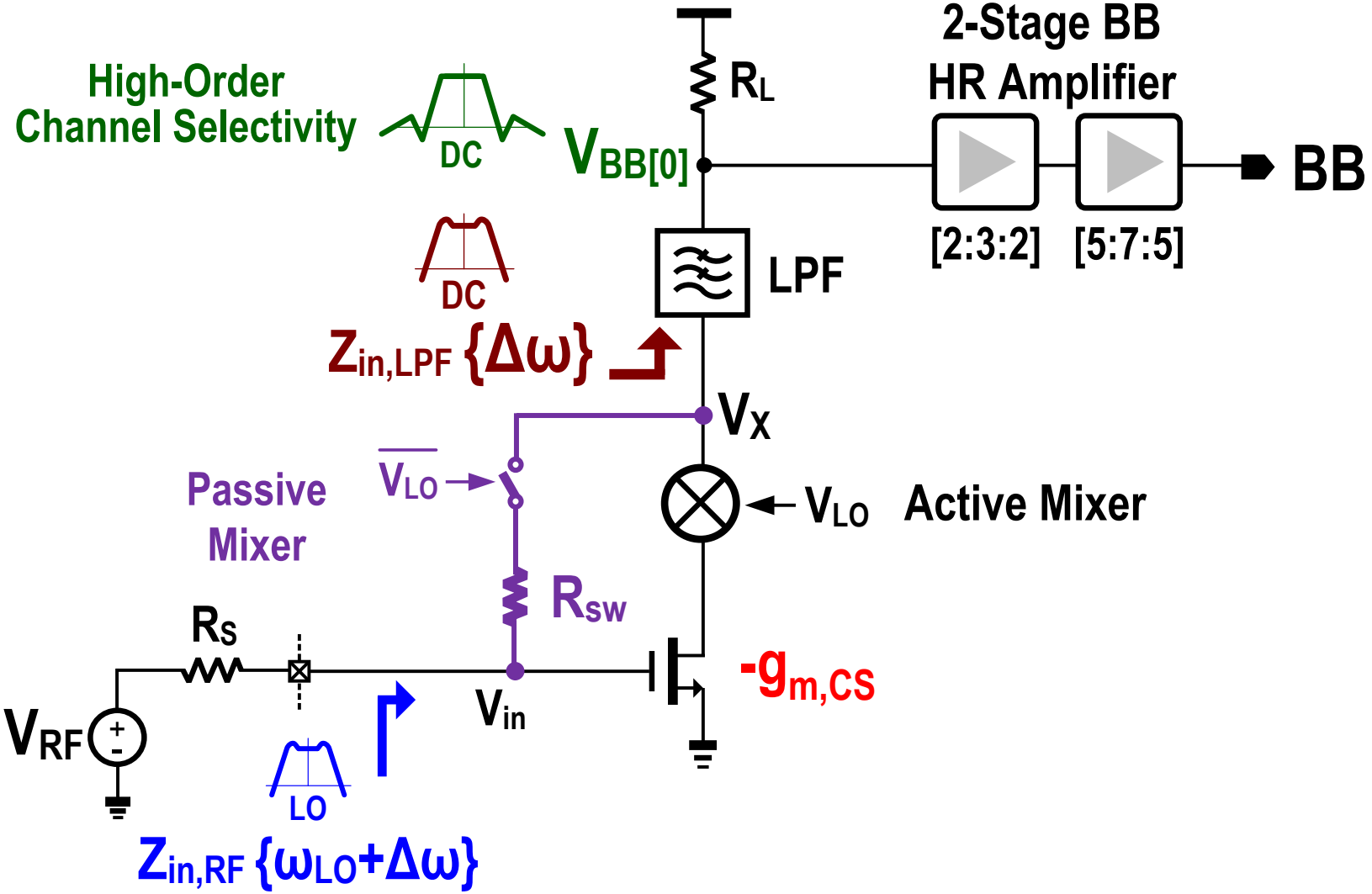
3 – Instituto Superior Técnico, U of Lisbon, Portugal

ISSCC 2014

Outline

- **Basic structure of the receiver**
- **Circuit details**
- **Experimental results**
- **Comparison with the prior art**

An RF-to-BB Current-Reuse Receiver

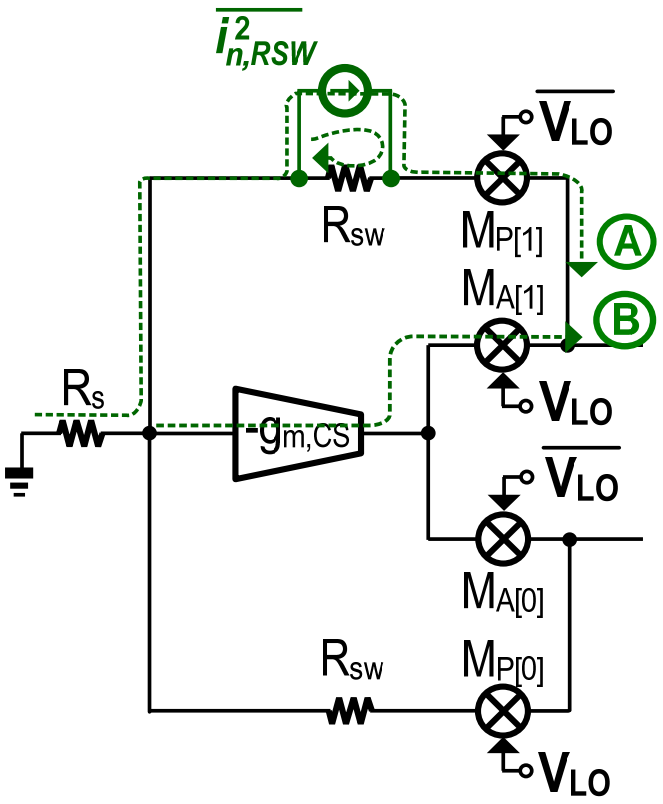


☑LO-defined input-impedance matching

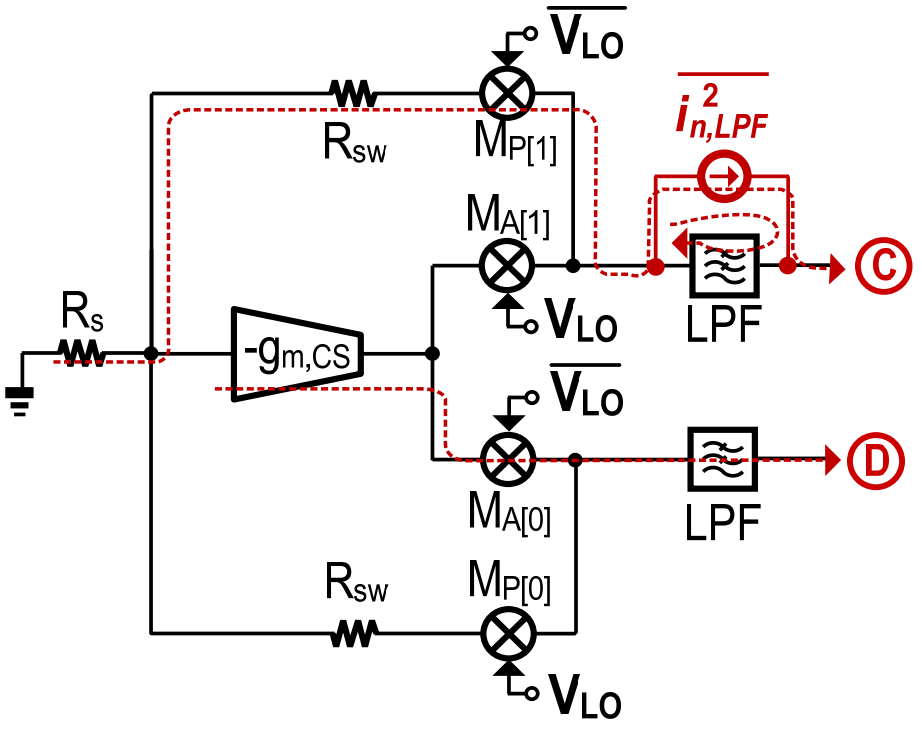
☑Bandpass @ V_{in} improves OB linearity ☑Input DC bias

Jointly Noise Cancellation of R_{sw} and LPF

Noise cancellation of passive mixer (R_{sw}) under $R_s g_{m,CS} = 1$



Noise cancellation of LPF under $R_s g_{m,CS} = 1$



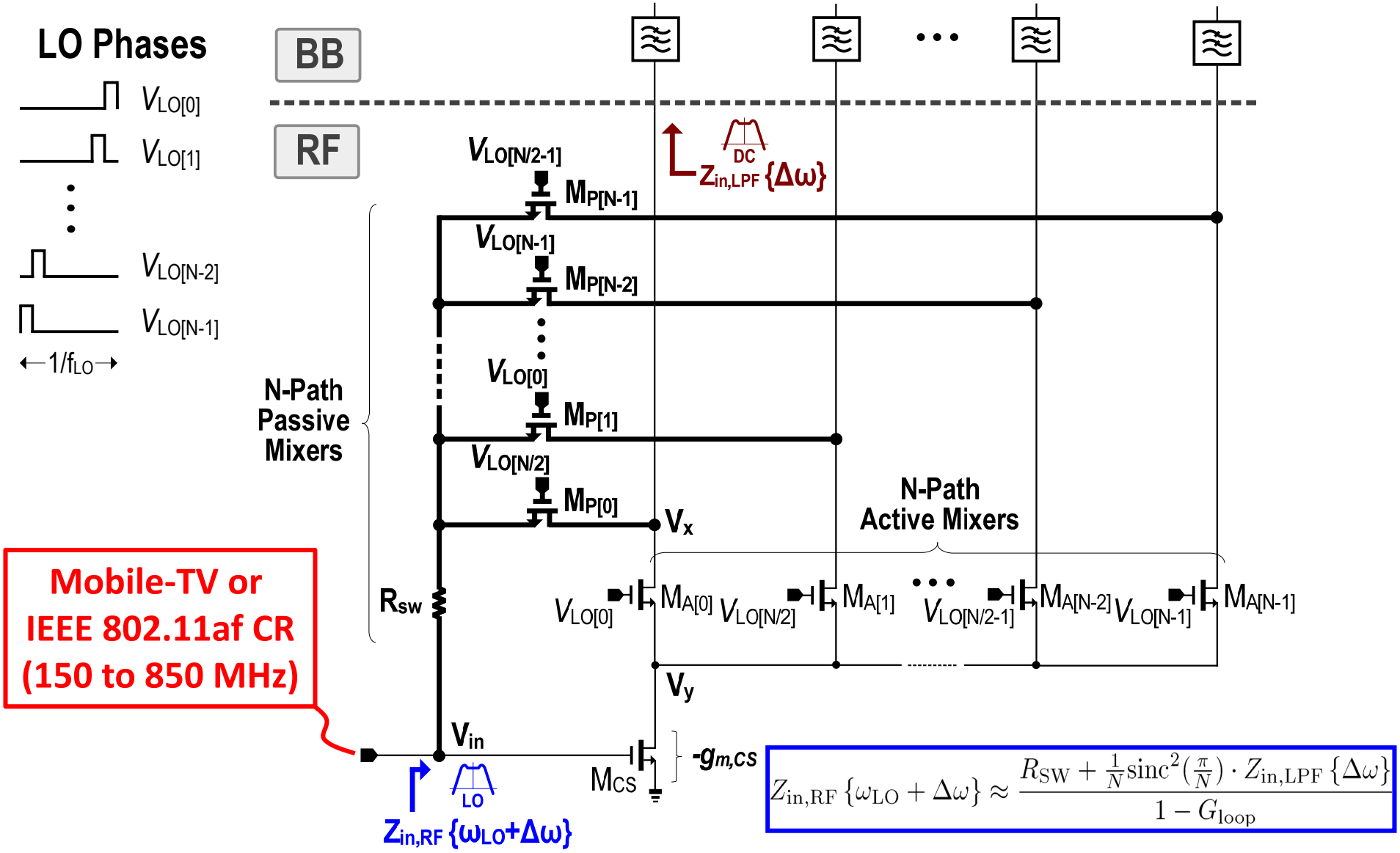
Ⓐ Path: $-k_1\overline{i^2_{n,RSW}}$

Ⓑ Path: $k_1\overline{i^2_{n,RSW}}R_s^2 g_{m,CS}^2$

Ⓒ Path: $k_2\overline{i^2_{n,LPF}}$

Ⓓ Path: $k_2\overline{i^2_{n,LPF}}R_s^2 g_{m,CS}^2$

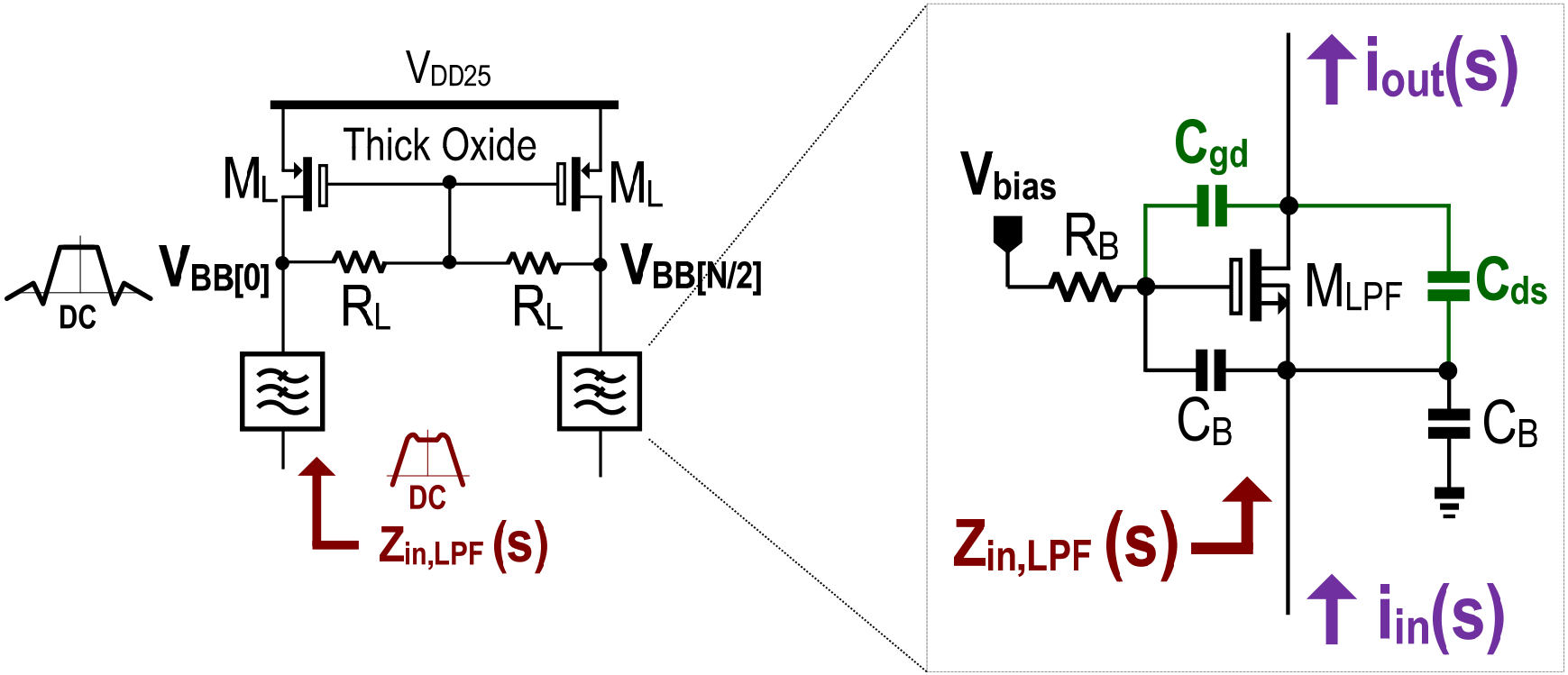
Parallel N-Path Active/Passive Mixers



$$Z_{\text{in,RF}}\{\omega_{\text{LO}}+\Delta\omega\} \approx \frac{R_{\text{SW}} + \frac{1}{N}\text{sinc}^2\left(\frac{\pi}{N}\right)\cdot Z_{\text{in,LPF}}\{\Delta\omega\}}{1 - G_{\text{loop}}}$$

- 8 paths for harmonic recombination at BB to enhance $HRR_{3,5}$

Single-MOS Pole-Zero LPF



2 Complex Poles

$$f_p \approx \frac{1}{2\pi}\sqrt{\frac{g_{m,LPF}}{C_B^2 R_B}}$$

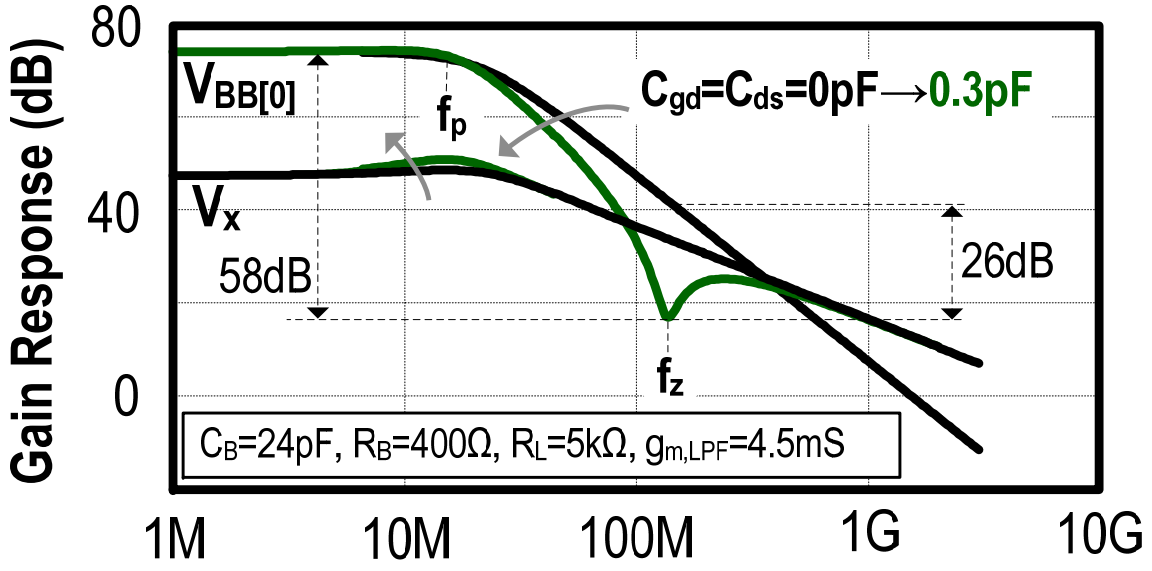
2 Stopband Zeros

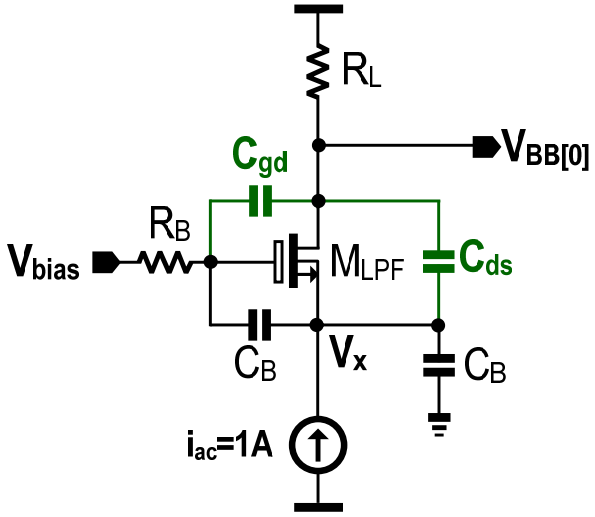
$$f_z \approx \frac{1}{2\pi}\sqrt{\frac{g_{m,LPF}}{R_B C_B (C_{gd}+C_{ds})}}$$

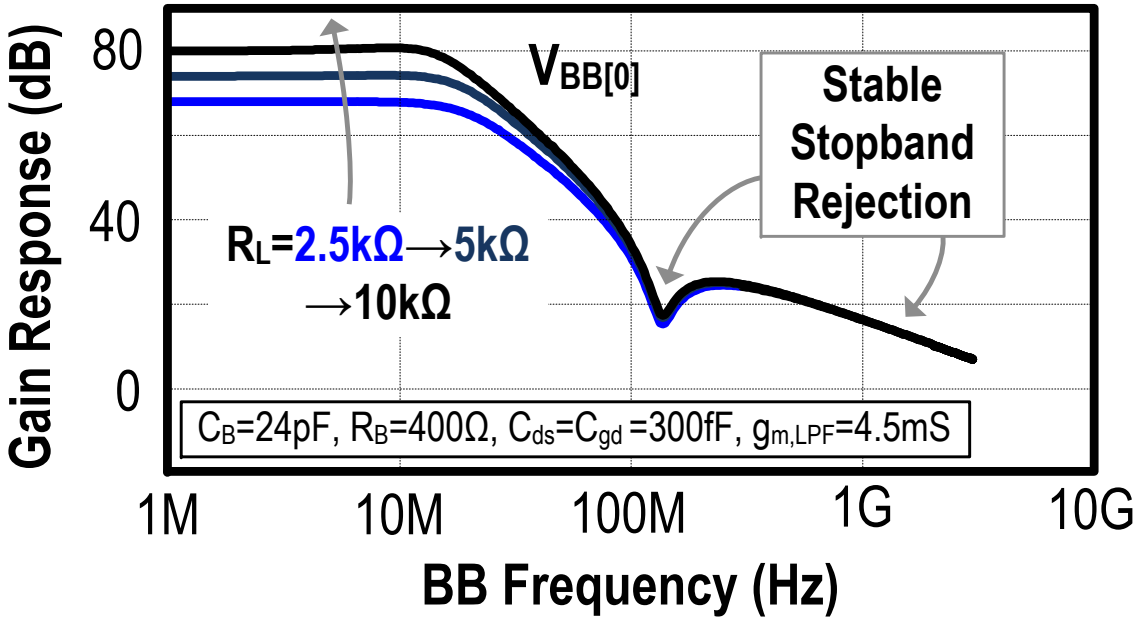
☑Noise of M_{LPF} is highpass at $i_{out}(s)$

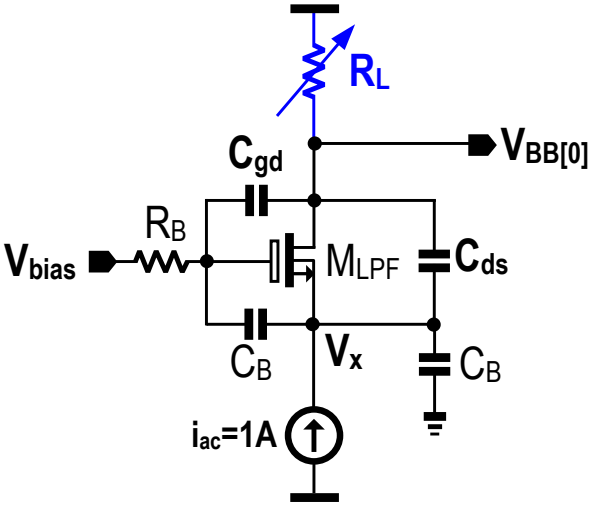
[J. Greenberg ISSCC'12] [A. Liscidini ISSCC'09]

LPF Characteristics Related with C_{gd}, C_{ds} and R_L



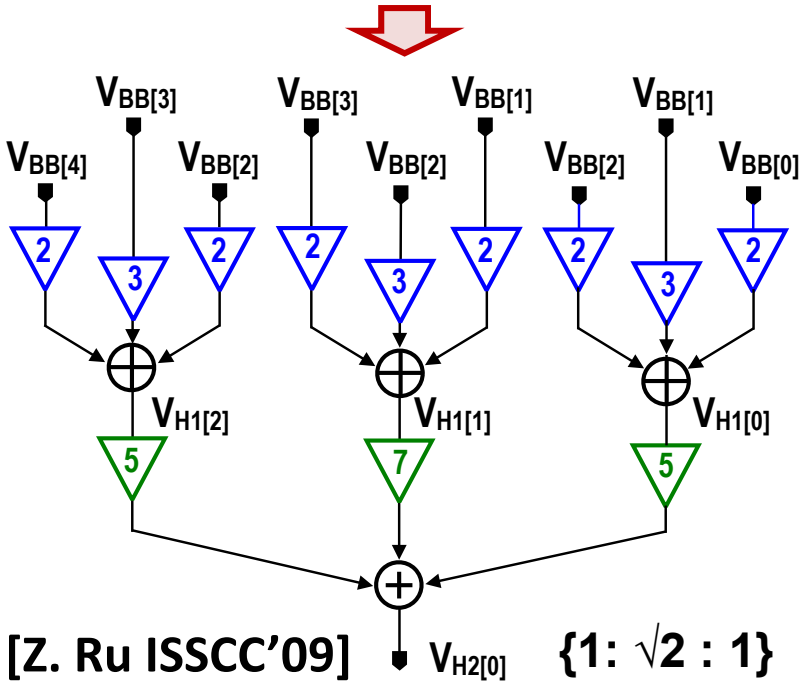




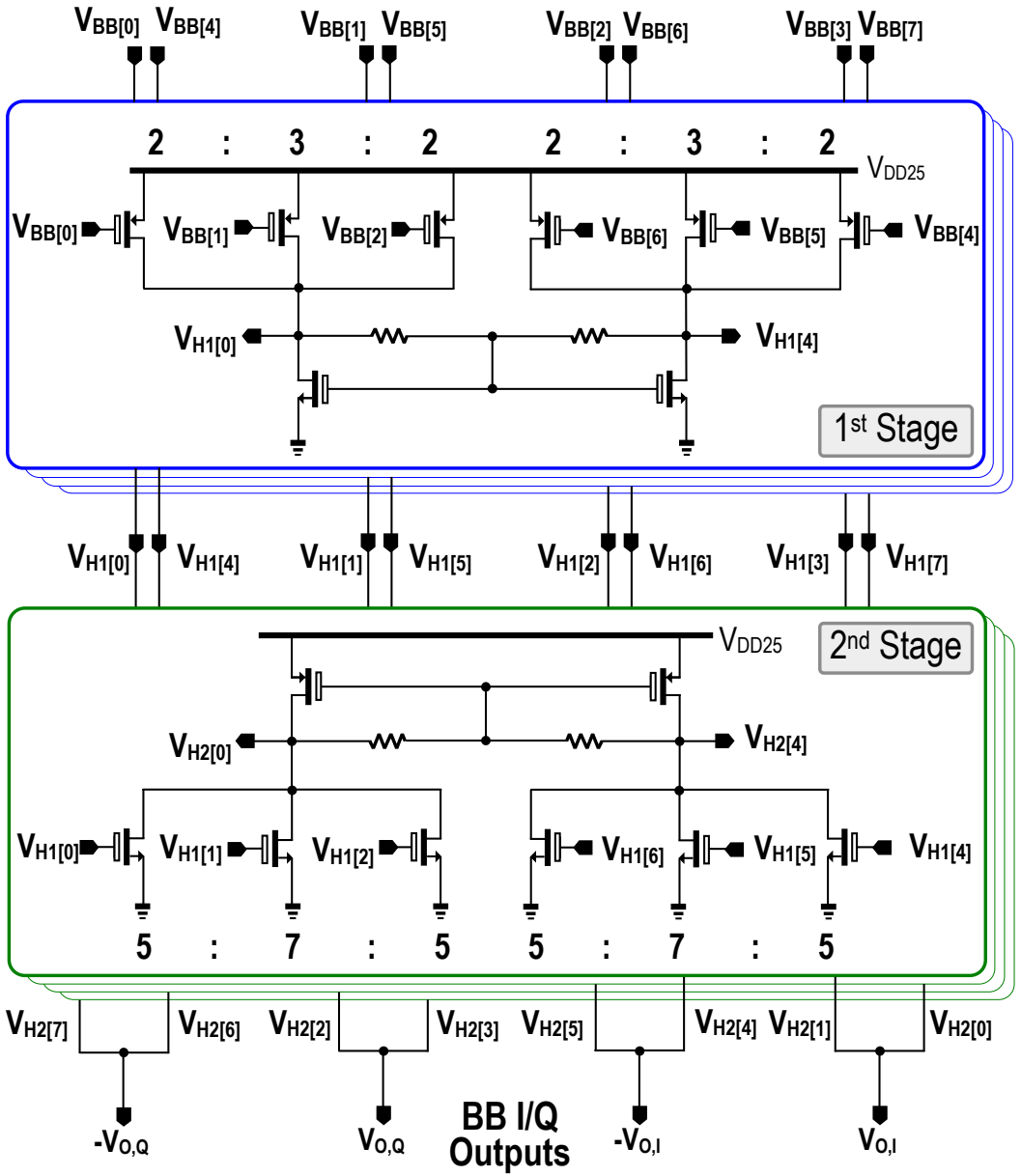


BB-Only Two-Stage HR Amplifier

8-Phase Outputs



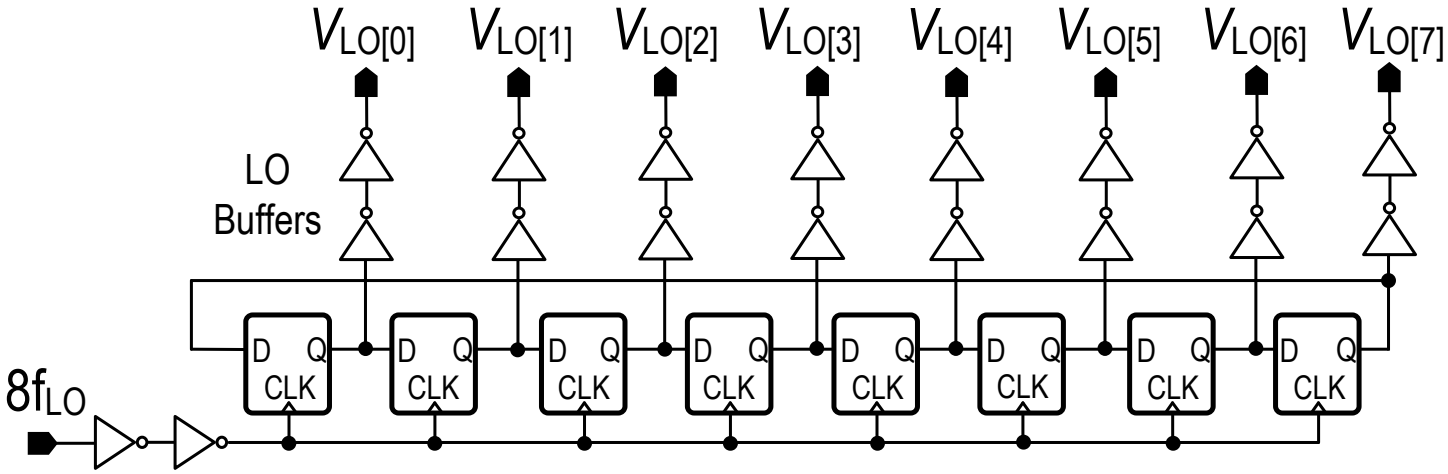
[Z. Ru ISSCC'09] $\{1: \sqrt{2} : 1\}$



Monte-Carlo Simulations

- Mean $HRR_{3,5}$ = 62 dB (ideal LO)
- $HRR_{3,5}$ is dominated by LO phase error

8-Phase 12.5%-Duty-Cycle LO Generator



~25 ps t_r & t_f (2% LO period at 850 MHz)

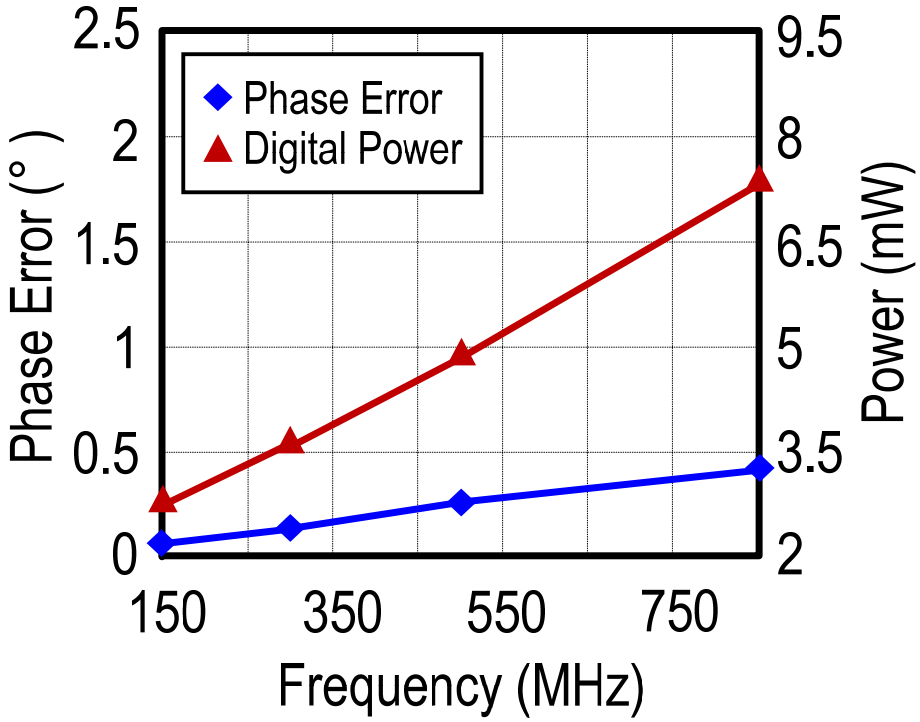
Simulated Phase Error:

σ= 0.045° @ 150 MHz

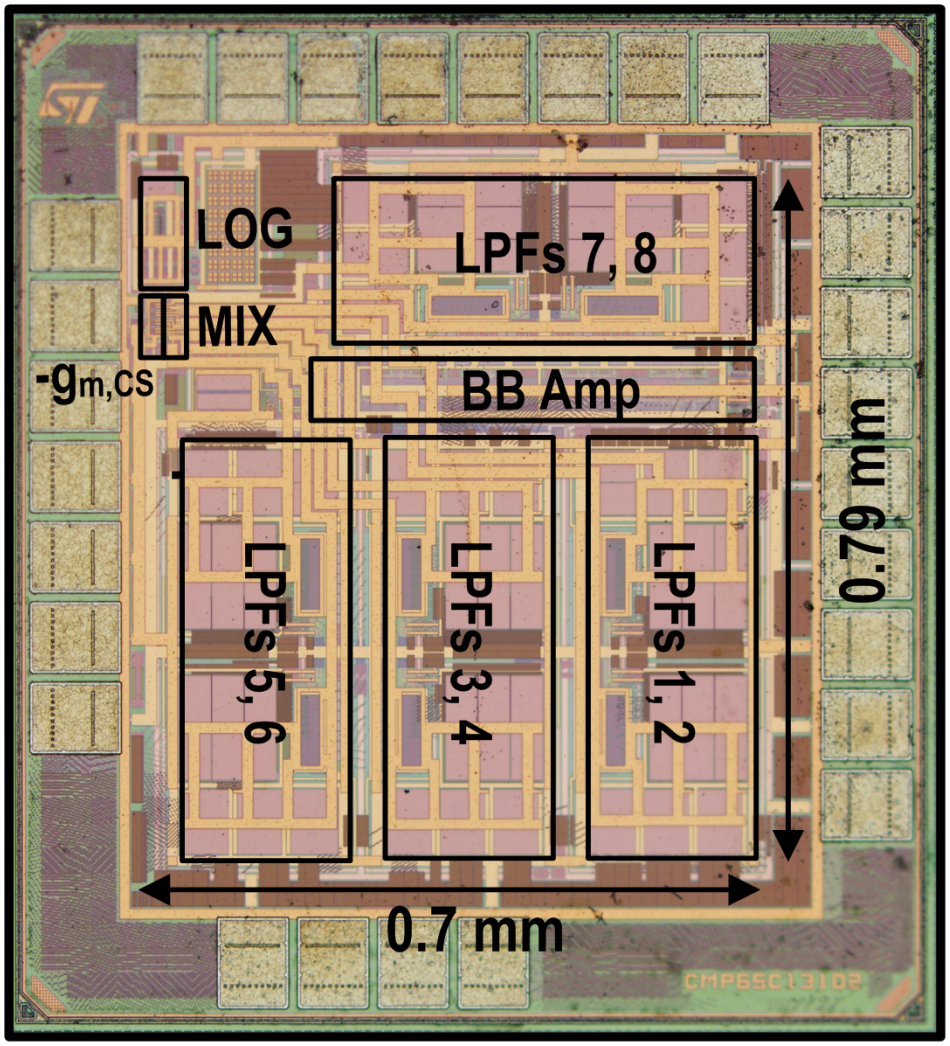
(Power = 2.8 mW)

σ= 0.4° @ 850 MHz

(Power = 7.5 mW)



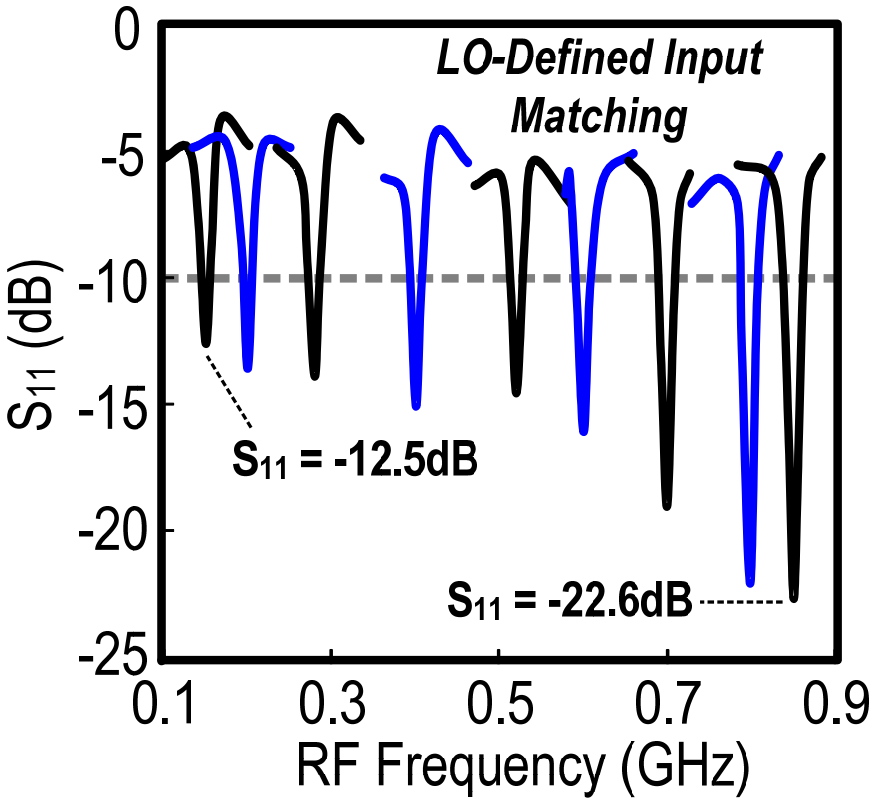
Chip Micrograph

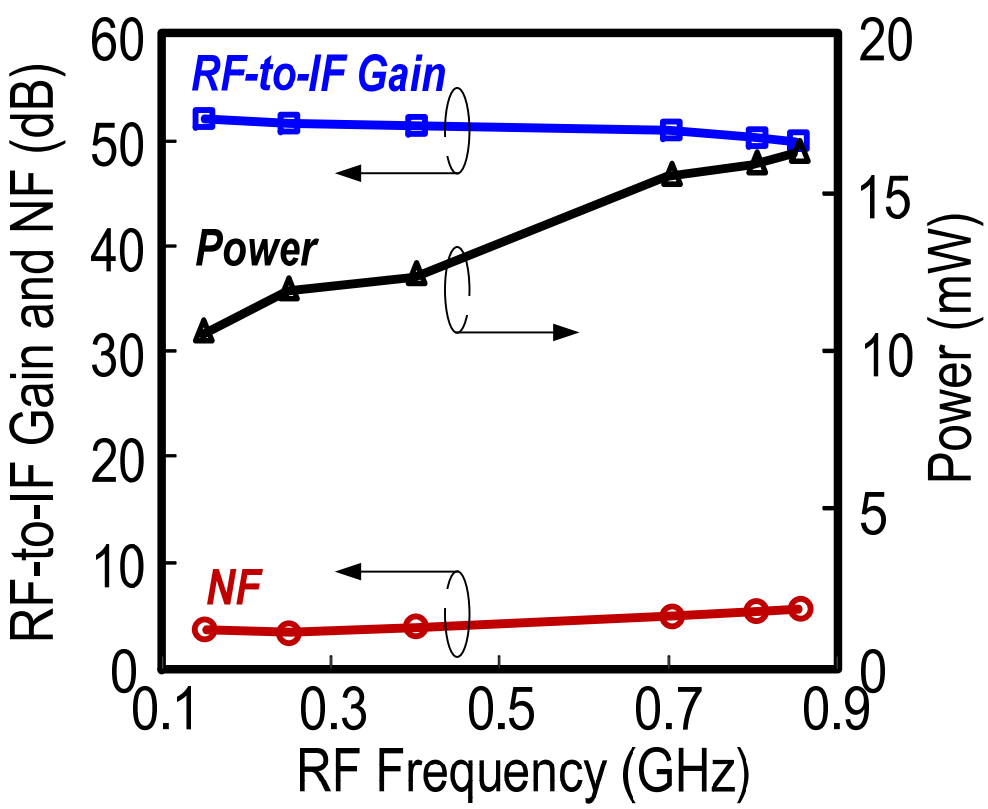


65nm CMOS	
CMOS	1.2V Thin-Oxide (RF)
	2.5V Thick-Oxide (BB)
CAP	MOM (C_B: 24pF x 16)

Active Area: 0.55mm^2
(excluding pads)

Measured S_{11}, Gain, Power and NF

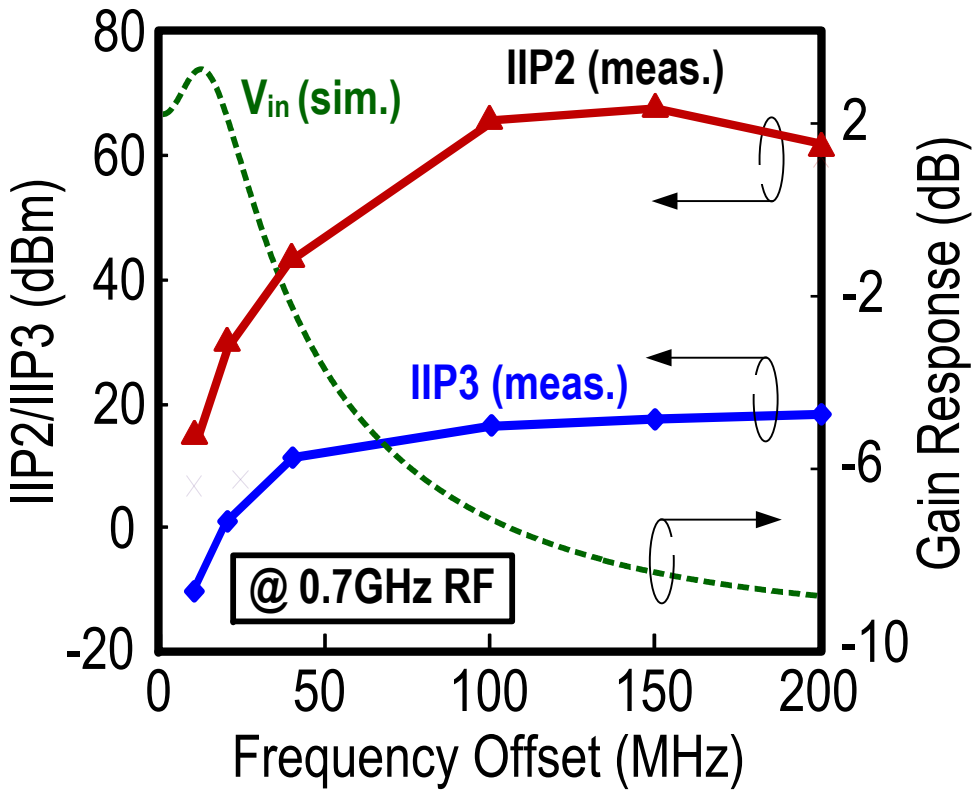


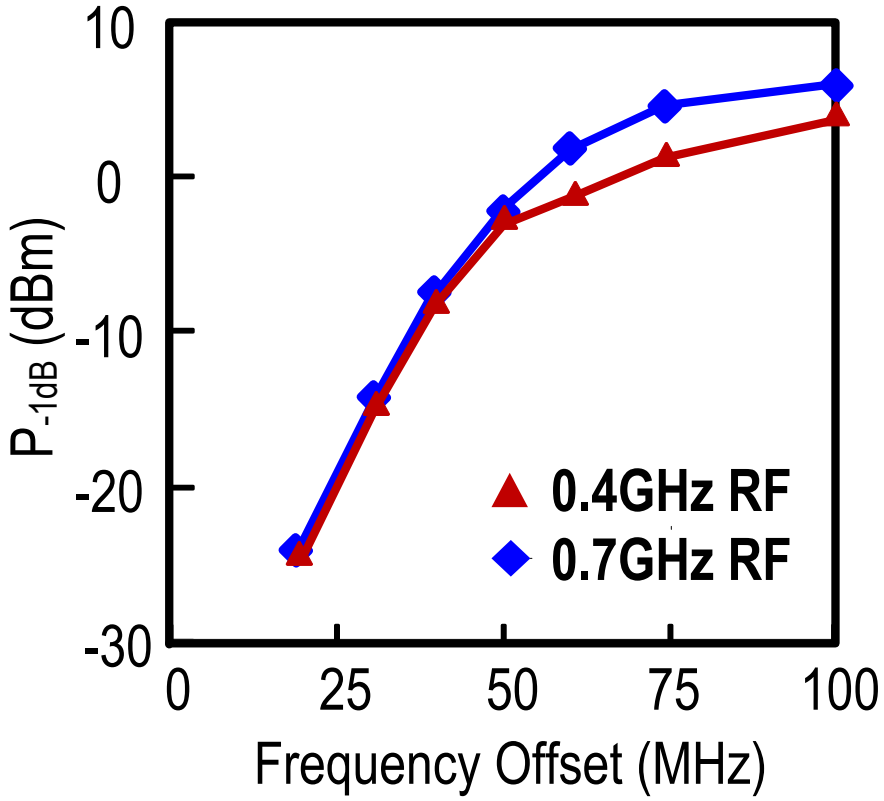


- **LO-defined narrowband S_{11}: <-12.5 dB**
- **RF-to-IF gain: 51 ± 1 dB**
- **NF: 4.6 ± 0.9 dB**
- **Power: 10.6 to 16.2 mW**

TV-Band
150 to 850 MHz

Measured IIP2, IIP3 and P_{-1dB}

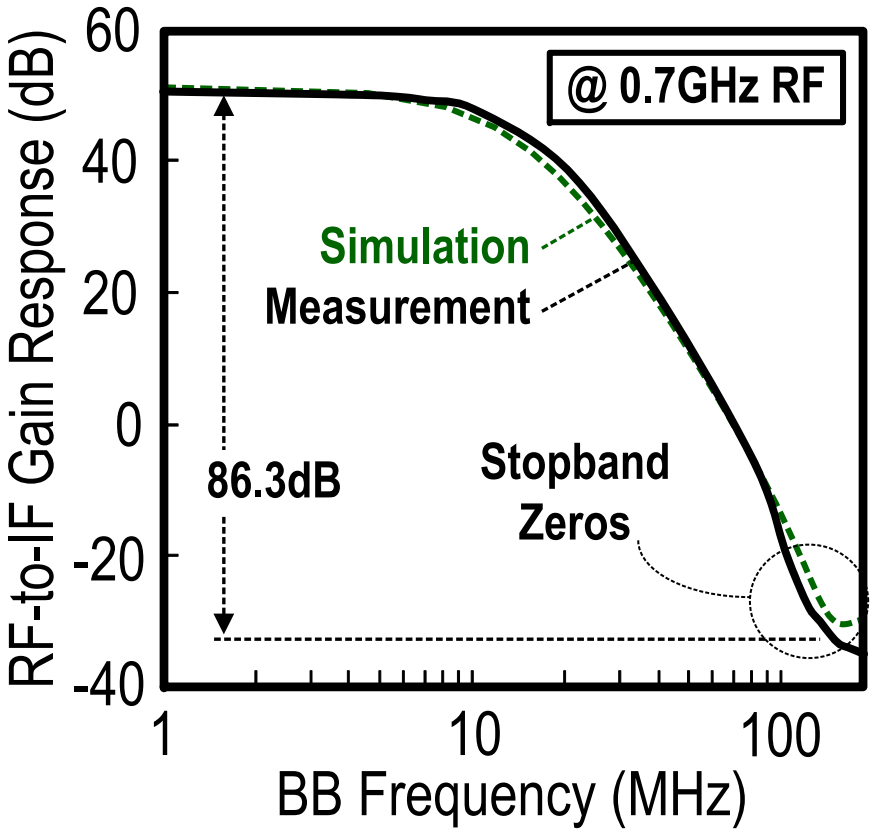


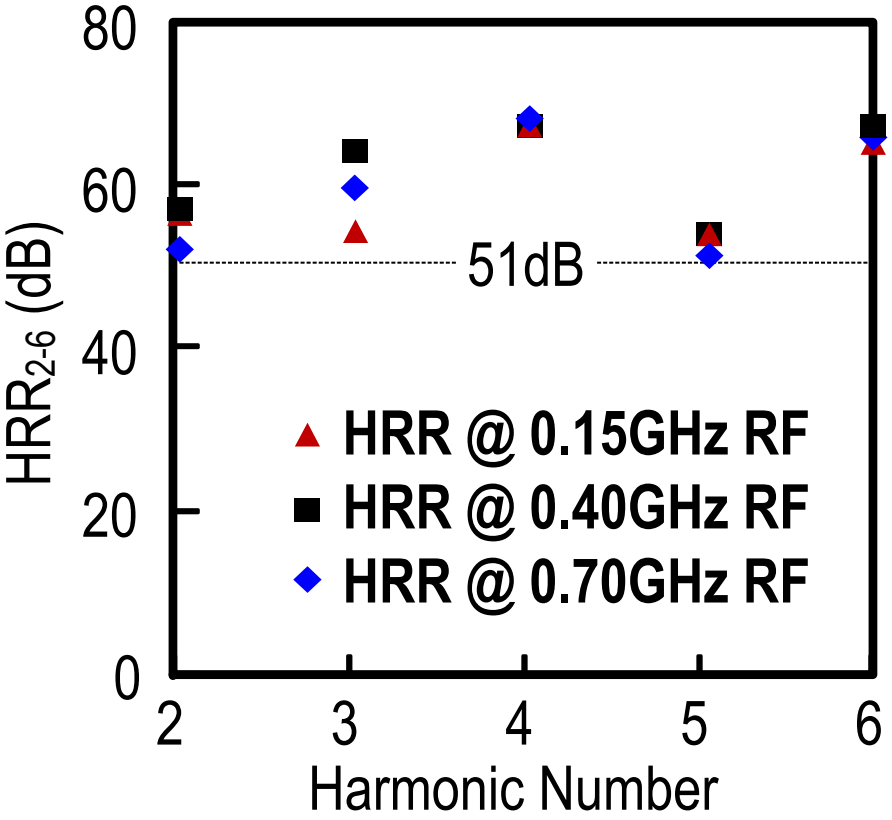


In-Band (-50dBm RF) & Out-of-Band (-25dBm RF) Linearity

- **IIP2 : +15 to +61 dBm** **2 tones: [$f_{LO} + \Delta f$, $f_{LO} + \Delta f + 1$ MHz]**
- **IIP3 : –12 to +17.4 dBm** **2 tones: [$f_{LO} + \Delta f$, $f_{LO} + 2\Delta f - 1$ MHz]**
- **P_{-1dB} : –25 to +2.5 dBm**

Measured IF Gain Response and HRR_{2-6}





- **BB bandwidth : ~9 MHz**
- **Stopband rejection : 86.3 dB @ 150 MHz offset**
- **HRR_{2-6} : >51 dB (from one randomly selected sample)**

Comparison with the State-of-the-Art

	This Work	JSSC'13	VLSI'13	ISSCC'12	ISSCC'09
Downconversion	**Active // Passive**	**Passive**	**Passive**	**Passive**	**Passive**
RF Input Style	Single-Ended	Single-Ended	Differential	Single-Ended	Differential
RF Range (GHz)	0.15 to 0.85	0.7 to 1.6 (8-phase path)	0.4 to 3 (8-phase path)	0.08 to 2.7	0.4 to 0.9
Power (mW) @ RF	**10.6 @ 0.15GHz** **16.2 @ 0.85GHz**	10~12 @ 0.7GHz 10~12 @ 1.6GHz	20 @ 0.4GHz 40 @ 3GHz	37 @ 0.08GHz 70 @ 2.7GHz	49 @ 0.4GHz 60 @ 0.9GHz
DSB NF (dB)	**4.6±0.9**	10.5±2.5	1.8 to 2.4	1.9±0.4	4±0.5
OB IIP3 (dBm)	**+17.4**	+10	+3	+13.5	+16
OB IIP2 (dBm)	**+61**	+26.6	+85 (calibrated)	+54	+56
External Parts	**Zero**	Zero	Transformer	Zero	2 Inductors and 1 Transformer
Active Area (mm^2)	**0.55**	2.9 (inc. VCOs)	~0.5 (from Fig.)	1.2	1
BB Filtering Style	**2 Complex Poles + 2 Stopband Zeros (Current-Mode)**	1 Real Pole (Passive-RC)	2 Real Poles (Active/Passive-RC)	2 Real Poles (Active/Passive-RC)	2 Real Poles (Active-RC)
$HRR_{3,5}$ (dB)	**>53, >51**	34, 34	70, 55 (calibrated)	42, 45	60, 64
BB Bandwidth (MHz)	9	20	0.5 to 50	2	12
RF-to-IF Gain (dB)	51±1	37	36	72	34.4±0.2
Supply (V)	1.2, 2.5	1.3	0.9	1.3	1.2
CMOS Technology	65 nm	65 nm	28 nm	40 nm	65 nm

Acknowledgments

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